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Department of Electrical Engineering
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Design and Implementation of Ultra-High Speed Automatic Flexible controlled SOA Equalizer with wide dynamic range.

Master Thesis

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Abstract

The research work described in this thesis focuses on the design, implementation and measurement of an analog ultra-high speed Semicondutor Optical Amplifier (SOA) equalizer. These activities are carried out in the framework of Erasmus+ internship program. Introducing optical switching technology, it has a prospective of offering flexibility, power efficiency, providing large capacity and fast response. In this thesis, the resolution of monitoring and equalization of the power for these fast optical switches is studied.

Not controlling the optical power, consecutive packets may suffer large variations in the signal power level. In an optical packet switching scenario, the dynamic performance of the packets duration is so short that analog circuit has to respond with enough speed to equalize the packets in this range of time. A fast optical switch usually use semiconductor optical amplifier (SOA) as switching gates, so their utility to equalize power variation of the packets becomes increasingly attractive due to its fast nano-scale response and adjustable optical gain.

The analog equalizer has to provide the correct bias current to an in-line SOA for an equalization of the packets in a specific sub-micron time response. This is accomplished by studying the mathematical concept of equalization up to fully design an analog circuit. Simulation of each stage as well as the whole circuit performance has been employed, showing promising results in the dynamics of the circuit, 100 ns response time. Moreover, the design of a Printed Circuit Board (PCB) layout to integrate different prototypes has also been exploited, where two prototypes has been presented: fixed-slope configuration (High-Speed Equalizer v1.0) and full-flexible configuration (High-Speed Equalizer 2.0). In the second prototype, programmable functionalities improving the flexibility of the equalizer can be supported, by updating the value of the slope and reference voltage of the scaling stage in 68 ms. Exploiting the capability of the prototype, two different regions has been tested, achieving a linear dynamic range of 10dB. Finally, a response time of 150 ns is reached by the full-flexible configuration with an average power consumption of 1.3W, where the penalty is introduced by the digital potentiometers.

Acknowledgments

I owe my gratitude to all people who contributed in the realization of my master thesis. I would like to first thank my supervisor, Dr. Nicola Calabretta for the opportunity to develop my master thesis in ECO group. I have learnt a lot under his supervision and guidance. His demanding and critic point of view always have pushed me to go beyond my limits, successfully achieving my first design from scratch. His insightful suggestions and help motivate me to keep going forward. Additionally, my acknowledgement to Dr. Salvatore Spadaro, who kindly put me in contact with this department, coordinating from Barcelona.

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Contents

Chapter 1

Introduction

1.1 Data centers: power consumption and the future of optics

Nowadays the extraordinary growth of the Internet in terms of number of users and thus bandwidth is a major factor. The last poll estimates around 3 and a half billion of global Internet users in the last year [1]. This exponential increasing is mainly driven from emerging applications such as streaming video, cloud computing and social networking. Then, there is a firm correlation between the increase in demand and the cost of bandwidth. This enforced necessity requires a demanding challenge to the networking of the data centers researching more efficient interconnection designs with high bandwidth and reduced latency. Besides, the total cost of computing, switching, and routing equipment is no longer controlled by its acquisition, but by its infrastructure: the cost of its powering, operation, maintenance, and administration. Since data centers power efficiency is less than 50%, this switching operation cost is already comparable to its acquisition expense. Today, individual switching chips consume about 20-40 pJ/switched bit [2]. The majority energy does not come from the switching circuits themselves, but rather by the electrical I/Os of the chips. For instance, I/Os transfer data to and from the VLSI switch chip can include considerable electrical interconnect interfaces. This leads to the necessity of increasing the performance-cost ratio of data switching and routing systems.

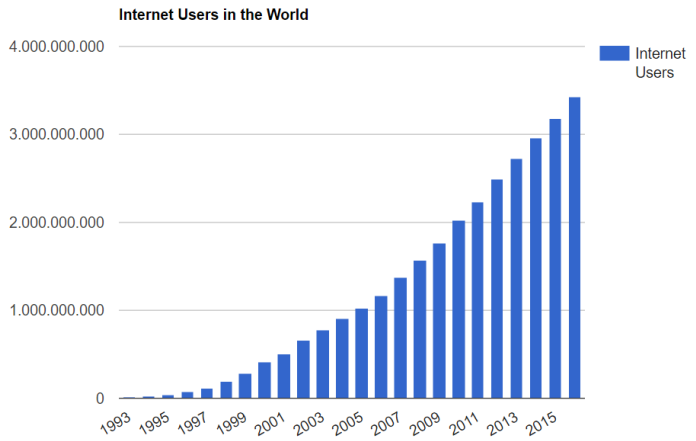


Figure 1.1: Number of global Internet users per year since 1993 [1]

These last years, the penetration of optical data links into communications systems has been widely accepted. Optical link directly integrated into switch chips would quit the use of electrical

chip I/O. This has a favourable trend since the integrated photonic links consume less power than the electronic ones, particularly passive switches (MEMS).

All in all, low-power silicon photonic connection can decrease the communication energy between chips and at the same time the I/O costs to and from the router. Figure 1.2 represents an approach of the rate of penetration of optics in terms of link distance and bandwidth. Optical links have reached bandwidth-meter performance beating 1Tb/s-m with single mode fiber. Following this trend, it suggests that in a near future, they can be expected to reach right to the chip-scale package on a PCB, working with link distances as short as one meter.

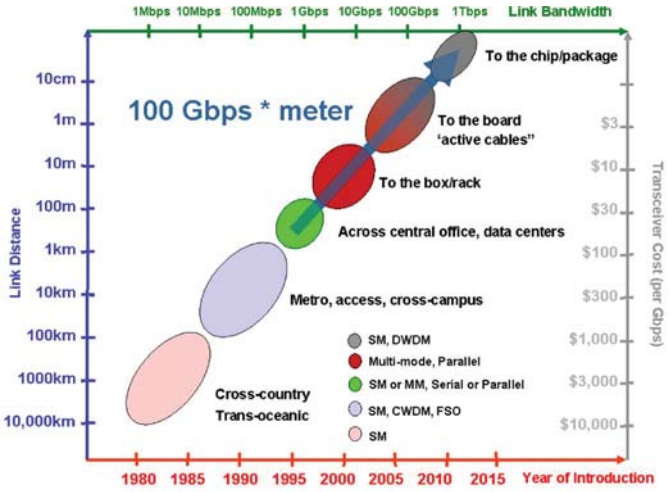


Figure 1.2: Penetration of optical links into communications [2]

Continuing the previous discussion, system limitations in data centers by means of power, bandwidth and density push the research field in rely on optical interconnect modules. Optical channels represent two main advantages ready to be exploited. First, an optical channel achieves higher bandwidth and response uniformity than its electrical counterpart, avoiding complex and cost of channel equalization. Second, the number of effective channels can be raised by using dense integration of photonic devices with silicon, in combination with WDM and multi-level encoding. So, each channel is not limited by the number of pins or timing complexities, improving significantly clock-recovery issue and lower its energy cost.

1.2 Optical data center network

Up to now, the traditional DCs are working with few capabilities in the optical domain such as amplification or wavelength de/multiplexing, but they still are in the electronic domain in terms of routing and switching. As it is mentioned in the previous section, the dramatic increase in demand for capacity needs to support that demand economically.

In an opto-electronic network the data is carried from point-to-point in the optical domain. For this network, fast-reliable opto-electronics components are required. First and foremost, let's start with some basic concepts related with the network. An optical channel is a light-path between two networks that can be routed through multiple intermediate nodes. Along that path one can find diverse elements such as optical line terminals (OLTs), optical add/drop multiplexers (OADMs), and optical crossconnects (OXCs) interconnected via fiber. Figure 1.3 represents the architecture of an optical network, also there are optical amplifiers (not shown in the scheme) to amplify the light signal along the fiber link.

OLTs are used at the end of a point-to-point link to de/multiplex wavelengths. One can find three main elements inside it: transponder, wavelength multiplexer and optical amplifiers.

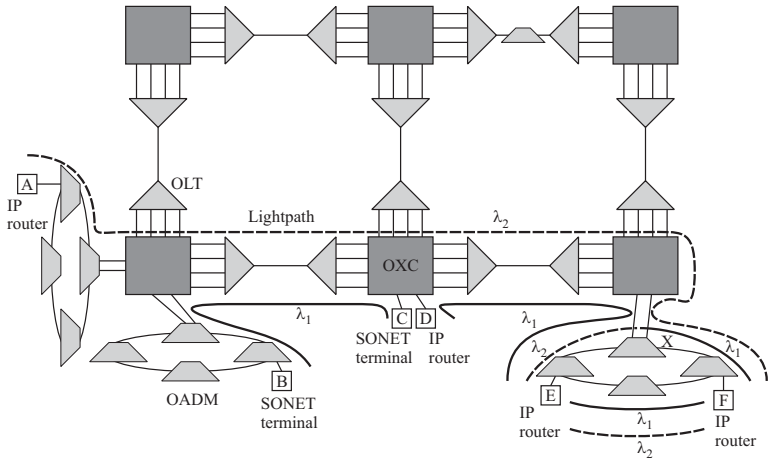


Figure 1.3: A wavelength-routing network with different elements, OLTs, OADMs, OXCs. The network provides lightpaths to its users, e.g, SONET and IP routers. [3]

OADMs afford an efficient performance for managing passthrough traffic in metro or long-haul networks. From a transmission point of view, OADMs consist mainly of an optical filters that impose spectral confinement of each WDM channel to a certain frequency band. Finally, OXC is also a key-element enabling reconfigurable optical networks, where the lightpath can be changed as needed. In actual scenarios, an OXC is pure electrical switch fabric but some researches are deploying a pure optical architecture. For instance, current optical add-drop multiplexers are based on electronics switches using O/E/O front cards. Novel researches propose OADMs based on optical packet switches that route transparently the data with different bit rates and formats at lower consumption.

1.2.1 Optical Packet Switching

Introducing optical switching technology, it has the prospective of growing the capacity and improving the power efficiency that we discussed before [4]. Optical slows switches MEMS-based has being included into data centers, providing the advantageous attribute of optical transparency. Nevertheless, tens of milliseconds of reconfiguration time has strictly involved to well-scheduled and long-lived tasks [5],[6]. Taking into account that the network traffic is becoming data-centric instead of voice-centric, the traffic source is bursty, it means that requires a lot of bandwidth from the network whenever it is active and very few bandwidth when it is not active.

In packet-switching, a technique called statistical multiplexing is implemented. Multiple bursty data is multiplexed together on a link, giving some time to a certain active streams. In order to facilitate the switching, a packet header -that contains the addressing information- is introduced to the payload in each packet. Then, the bandwidth is improved but occurs some side-effects. If more streams are active simultaneously than the available bandwidth on the link, some packets must be buffered until the link becomes free again. By this time, DCs use an electronic packet switching due to its bandwidth efficiency and ability to support diverse services. Nonetheless, novel researches are focusing in the packet switching concept into the optical domain. It is plenty of research into optical packet switching during the last years, however, header processing and control deployed in the all-optical plane is still many years away [7]. Being more realistic, OPS using an electronic control plane is a short-term concept. In the opto-electronic approach the optical packet contains an optical label attached to the payload that is read and compared electronically with a look-up table, meanwhile the payload is totally transparent through the switch (see Fig 1.4).

That interesting road-map of the optical transport network can be illustrated in the next generation on data centers. The fast optical switches give more meaning to packet-switching

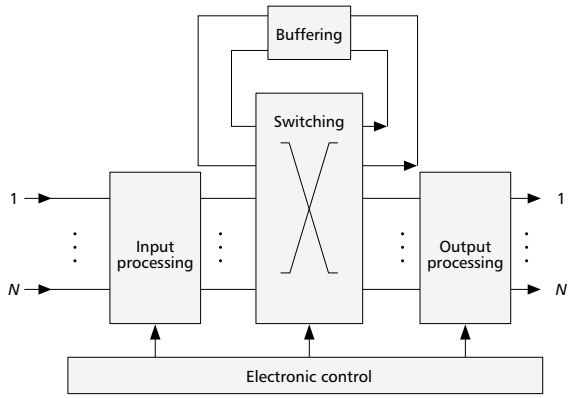


Figure 1.4: A schematic of a generic structure of the OPS [8]

technique allowing it for on-demand resource utilization and flexible connectivity. On the contrary of its electronic counterpart, the fast optical switch is becoming a feasible candidate. In despite of its promising future, the implementation of the fast optical switches supporting packed-based operation is facing different challenges.

1.3 Equalization on fast optical switches

Fast optical switching, in support of the packet-based operations, imposes the resolution of the next problem: the monitoring and equalization of the power. In the wide range of optical packet router architectures, the power experiences different variations from non ideal passive and active optical devices. Not controlling the optical power, the perturbations between consecutive packets at the input/output of a switch may reach 10 dB difference. In consequence, the receivers' specifications on the dynamic range and the optical switch are continuously pushed. That fast optical switches mainly use semiconductor optical amplifier (SOA) as switching gates, so ca be also employed to equalize packet/burst power variation.

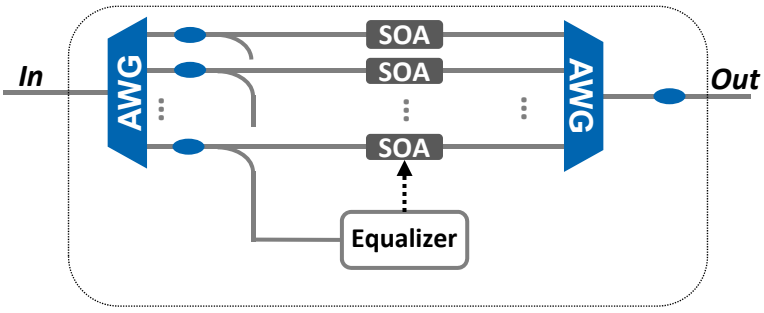


Figure 1.5: Schema for power equalization

The first schema of equalization is presented in Figure 1.5. Exploiting SOA technology, it can provide an adjustable optical gain for power equalization. Hence, a closed-loop with the equalizer fixes a constant current to an SOA providing the necessary optical gain to the packets. The equalizer has to convert the optical power into electrical signal such as an output current, in section 1.4 is introduce the two main possibilities (analog/digital) for implementing the device.

1.3.1 Specifications for a fast power equalization system

The main sources of power alterations by crossing different optical paths are the following:

- Polarisation dependency of the components.
- Non ideal flatness of the pre-amplifiers (EDFAs).
- Non ideal insertion loss in passive components(couplers, AWGs...)

Figure 1.6 shows a general power budget of an optical link. Different elements during the transmission affects to the power of the link, the receiver sensitivity and the link loss leave us a margin where sometimes is not possible to achieve. With any correction of the previous perturbations, the power dynamics could reach values which can make infeasible any optical matrix.

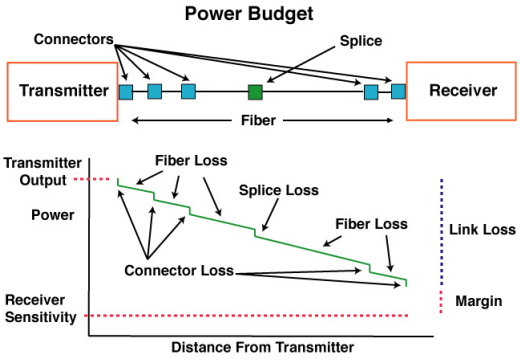


Figure 1.6: Evolution of a power budget in an optical link [9]

Several power equalization methods based on control feedback loops have been proposed previously [10], [11], [12]. However, these methods do not provide satisfactory dynamic performance in an optical packet switching (OLS) scenario as the duration of a packet and the time between consecutive packets is so short that a feedback loop is unlikely to respond with sufficient speed to provide the power equalization both for an individual packet and between packets.

1.4 Specifications of the system

Recent article demonstrate a novel optical label switching OADM prototype able to transparently switch data with some promising results [13]. It is still in developing and this thesis is part of that project. Figure 1.7 depicts the whole system of the (OLS) OADM node and the packet format.

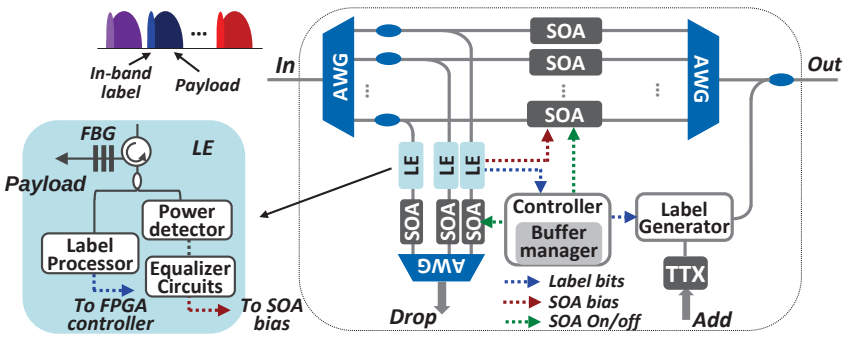


Figure 1.7: Schematic of the OLS OADM node [13]

By means of the AWG the WDM channels are first demultiplexed and divided by a coupler into a drop arm and pass-through arm. In the continue arm, the wavelength is amplified by a semiconductor optical amplifier (SOA) which is managed by an electronic controller in nano-seconds scale. In the drop arm, an external module called Label Extractor is in charge to process the optical label. The payload is separated from the label by a narrow band fiber brag granting (FBG). The power extracted is fed into a coupler and divided into two parts. On one hand, the extracted label in processed by the Label Processor to recover the RF tone label bits. On the other hand, a real-time high speed power equalization is required to bias the SOA with the correct current. In the add arm, the controller configures the fast tunable transmitter and the Label Generator to transmit the packets with the corresponding labels stored in the buffer.

The challenging problem to solve is the design of the mentioned fast per-channel power equalization for the OLS OADM in order to achieve the most restrictive specification: response time.

Figure 1.8 depicts a qualitative representation of the issue. The optical label is filtered out by using a FBG with 3dB-bandwidth of 6GHz. The blue graph is a portion of in-band optical label power used to the real-time monitoring and equalization. The red graph represents the packets passing through node-to-node, synchronous slotted operation with fixed packet duration of $2\mu s$. Finally, the last graph points out the guard time which is the maximum time allow to equalize the packets without any penalization.

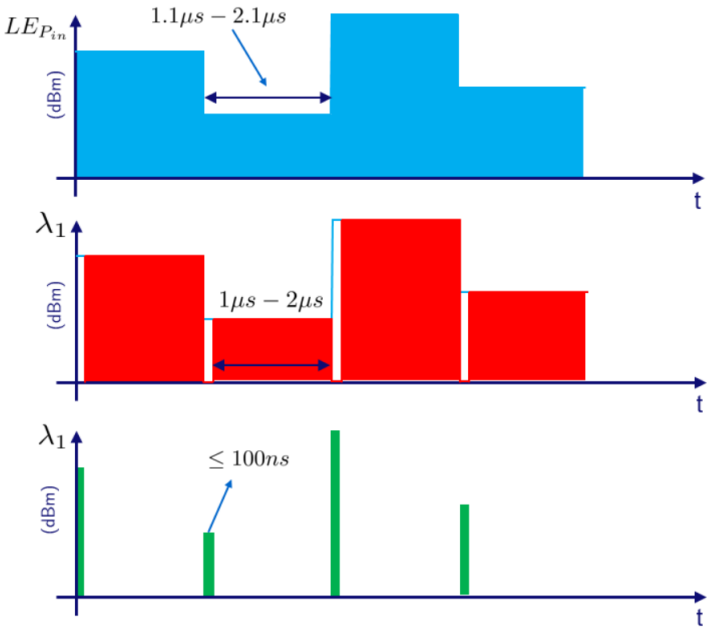


Figure 1.8: Representation of different paths of the optical signal in time

Up to that point of the design stage, where the output response is well-defined, the implementation of the signal is discussed. There is two different paths to solve the problem, either digital design or analog design. For a digital design, a feasible alternative is to use a digital system such as a FPGA to acquire all the curve in a look-up table and a couple of DACs in order to provide the bias current [14]. However, the scalability of the system is reduced to the number of DAC available in the FPGA. Another drawback is the cost of each high-speed DAC as well as the latency introduced to the system. For an analog design, it is the best candidate in order to achieve the constrains of the system. Scalability is an advantage since the circuit could be reproduce for each channel at a low cost. Nevertheless, the price to pay is the restriction in the dynamic range of the equalizer, we are limited in the linear part of the SOA transfer function. Finally, we summarize the main points in the table 1.1. The cost and scalability are the most attractive ideas for a future implementation of multiple channels of the OADM or optical switch.

Table 1.1: Comparison between FPGA implementation and Analog implementation

	Analog Design	Digital Design
Cost	IC + PCB	FPGA + DACs
Scalability	# of PCB	# channels of the DAC
Flexibility	Non-flexible	Full flexible
Response time	$\leq$ 100 ns	100ns$\leq$t$\leq$ 1μs

1.5 Thesis Objectives

The objective of this thesis is to study a feasible implementation for fast-per-packet power equalization for an optical switch. Starting from the mathematical concept of equalization up to the fully design of an analog circuit, where many steps were necessary to make possible such idea. This is accomplished by studying the different stages providing the correct bias current to an in-line SOA for an equalization of the packets in a specified sub-micron time response.

- The first challenge is to select the optimal components to achieve the specifications of the system in terms of bandwidth, sensitivity, rising/falling time and power consumption.
- The second challenge is to perform simulations in order to study the behaviour of each component as well as the whole circuit performance.
- The third challenge is to design a PCB layout to integrate the different prototypes and test it afterwards. Moreover, the components are in-house assembled by using re-flowing technique.
- The fourth challenge is to characterize the devices and to compare it with the simulation stage. This stage also includes the debugging of the PCB and tuning of the passive components.
- The fifth challenge is to proof the equalization by testing the device with different experimental setups.

1.6 Thesis Outline

The thesis is structured as follows. In Chapter 2, the theoretical design of the equalizer is presented. The choice of each stage is motivated by explaining its mathematical principles. Chapter 3 introduces the simulation of the circuits to analyse the viability of the circuit with the selected components. The performance of the circuit in terms of biasing, stability and transient analysis is reported. In Chapter 4, the design of the PCB layout is described in detail. From the footprint of the components up to the different layers of the PCB are introduced. Chapter 5 presents the characterisation of the devices, where the results are compared with the simulations and the mathematical equations. In addition, for one of the prototypes, a user-interface is explained and the connection establishment time is also reported. In Chapter 6, characterisation of an SOA and different equalization setup are present. The analog circuit has to be designed according to the transfer function of the SOA. Experimental demonstration of the equalization is performed showing the issues of the system. The thesis concludes with Chapter 7, where the main results are summarized and a future outlook is proposed.

Chapter 2

Design of High-Speed Equalizer

In this chapter, the concept and demonstration of equalization is introduced. As described in Chapter 1, fast optical switching still needs the monitoring and equalization of the packet's power. In the following, the equalization operation is described in the section 2.1, explaining the mathematical model and two different approaches (linear and logarithmic). A preliminary description of the complete system, where it is part of *EU LIGHTNESS* project, is described in the section 1.4, followed by the implementation of the device (analog or digital domain). The circuit design, including the key aspects of the components and each stage, is introduced in the section 2.2. Finally, the whole design of the circuit is analysed and represented in the section 2.3.

2.1 Equalization operation

This section describes the fundamentals of the equalization. Defining the behaviour of the system to concordantly design the circuit is the basics of any good analog design. Then, the next step is to focus in the response of the circuit, how the output signal of the circuit should be in order to equalize the different packets in a wide dynamic range. To do so, the transfer function of an SOA have to be analysed. Figure 2.1 shows a typical curve of an SOA gain. The y-axis are shown in dBs, meanwhile the x-axis are shown in milliamperes.

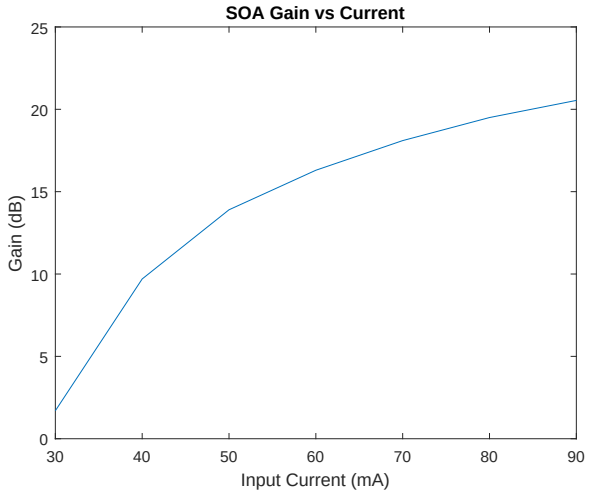


Figure 2.1: Transfer function of an SOA

From one side, the gain in dBs is proportional to the bias current up to certain point that

starts to grow non-linearly. The ideal equalizer should track completely the curve depending on the input power that the photo-diode detects, however, analog circuits simply can not implement a second order system in a trivial methodology and over with that demanding time response. Nevertheless, the transfer function is linear in a range of 10dBs. The mathematical equation that describes a straight line is :

$$G_{SOA_{dB}} = m \cdot I_{bias} + G_{0_{dB}} \tag{2.1}$$

where m is the slope (dB/mA) and $G_{0_{dB}}$ is the y-intercept.

From the other side, equalization is defined as keeping equal the output power of the optical link for any input power. Since we are limited by the linear region of the SOA, some boundaries have taken into account. Moreover, working on dBs has the advantage of adding or subtracting rather than multiplying or dividing. The output power of the packet follows:

$$P_{out_{dB}} = G_{SOA_{dB}} + P_{in_{dB}} \rightarrow G_{SOA_{dB}} = -P_{in_{dB}} \tag{2.2}$$

Equation 2.2 shows the necessary gain to fully equalize the incoming signal, where the reference power is set to 0dBm. Being more specific, what we want in a range of 10dB of input power is to maximize the lower power and maintain the higher power at the same level. This can be described as:

$$G_{max_{dB}} = P_{max_{dB}} - P_{min_{dB}} = 10dB \tag{2.3}$$

$$G_{min_{dB}} = P_{max_{dB}} - P_{min_{dB}} = 0dB \tag{2.4}$$

Relating equation 2.3 and equation 2.2 the gain of the SOA must trace:

$$G_{SOA_{dB}} = (-P_{in_{dB}} + P_{min_{dB}}) + G_{max_{dB}} \tag{2.5}$$

Substituting equation 2.5 into equation 2.2, the result is always the maximum input power at the output of the SOA.

$$P_{out_{dB}} = G_{SOA_{dB}} + P_{in_{dB}} = (-P_{in_{dB}} + P_{min_{dB}}) + G_{max_{dB}} + P_{in_{dB}} = P_{max_{dB}} \tag{2.6}$$

The final step is to associate the bias current with the gain. This is accomplished by substituting equation 2.1 to equation 2.6.

$$I_{bias} = \frac{1}{m}\left[(-P_{in_{dB}} + P_{min_{dB}}) + G_{max_{dB}}\right] - \frac{1}{m}G_{0_{dB}} \tag{2.7}$$

As shown in equation 2.7, the bias current is proportional to the input power in dBs, where depending on the characteristics of the SOA, the slope m, y-intercept $G_{0_{dB}}$ and the maximum linear gain $G_{max_{dB}}$ are variables that can be different.

Figure 2.2 shows what we have expressed before. The first graph represents the gain function depending on the input power, in that case, a range between -30dBm and -20 dBm are chosen since it is a feasible value for a data center environment (after a 90/10 coupler). The second graph shows the gain provided by the bias current, this is the linear part of the transfer function shown in the Figure 2.1. Finally, the last graph depicts the output power once the SOA has equalized the incoming signal.

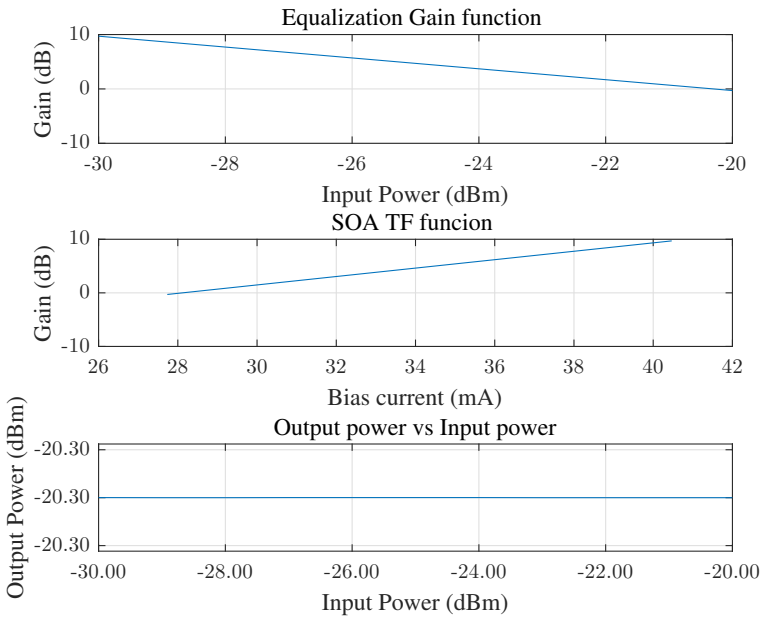


Figure 2.2: Equalization fundamentals on logarithmic range

The presented analysis was for the statics of the equalizations. Nonetheless, another solution was also considered. The main idea is to analyse a transfer function of an SOA in a linear scale, in other words, the gain shown watt-per-watt rather than dBs. Then, a mathematical analysis is repeated but considering the consequences of working in linear. Figure 2.3 shows the same transfer function than the Figure 2.1 but in linear scale.

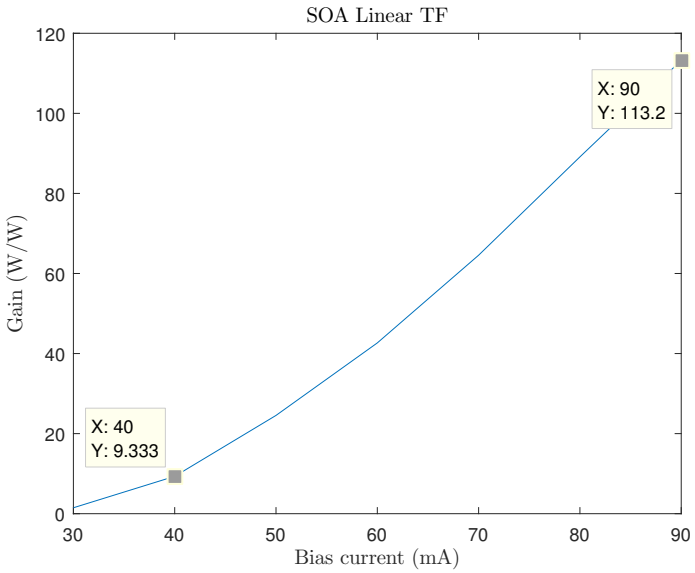


Figure 2.3: Transfer function of an SOA

As the same case as before, the SOA only has a straight-line behaviour up to a certain point of the curve, so the approximation is a straight-line equation:

$$G_{SOA} = m \cdot I_{bias} + G_0 \tag{2.8}$$

but the bias current is proportional to the gain in watt-per-watt. Remarking that the equalization procedure is quite different from the previous one since there is logarithmic scale any more. The output power of an SOA is delineated by a multiplication instead of a sum:

$$P_{out} = G_{SOA} \cdot P_{in} \rightarrow P_{out} = \frac{1}{P_{in}} \tag{2.9}$$

Setting the same boundaries, the range of the input power follows 1 up to 10 (it is the equivalence of 0dB and 10dB). Any case, equation 2.10 shows the general expression of the gain.

$$G_{SOA} = \frac{P_{min}}{P_{in}} \cdot G_{max} \tag{2.10}$$

One can realize that substituting equation 2.10 into equation 2.9 the result is exactly the same than the equation 2.6

$$P_{out} = \frac{P_{min}}{P_{in}} \cdot G_{max} \cdot P_{in} = P_{max} \tag{2.11}$$

The final step is related the equalization formula with the bias current of the SOA, so taking equations 2.8 and 2.10:

$$I_{bias} = \frac{1}{m}\left[\frac{P_{min}}{P_{in}} \cdot G_{max}\right] - \frac{1}{m}G_0 \tag{2.12}$$

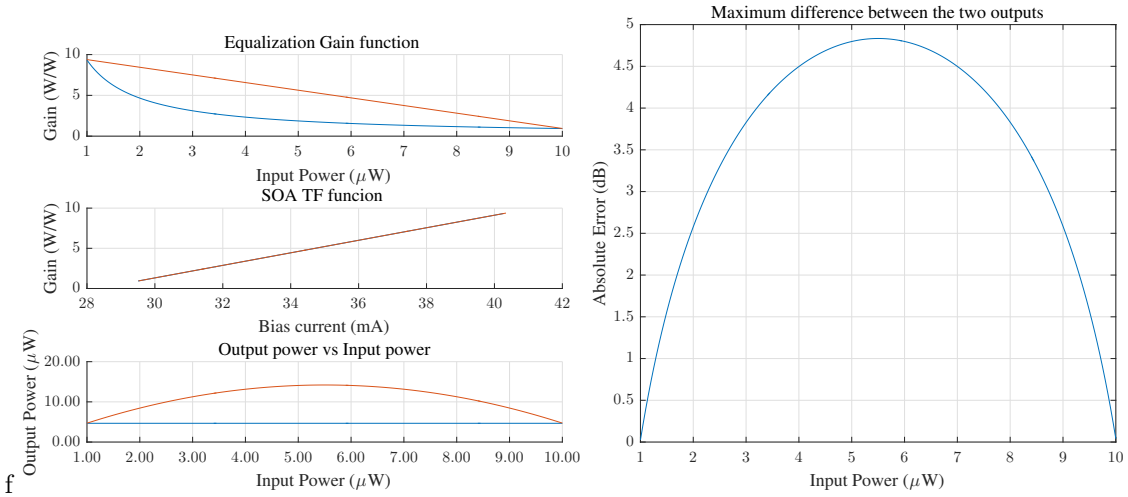
Figure 2.4a represents equalization in terms of linear scale. Also, it is included a case which shows what occurs when the basic design it is not well-implemented. Firstly, the blue plot is the representation of the linear equalization. The first graph depicts the necessary gain to equalize the input power correctly, it follows the equation 2.10. The second graph draws the straight-line behaviour of the SOA against the bias current. At last, the output power stays constant for all the range of the input power.

Regarding the red plot, it demonstrates the error committed during the design of the equalizer. The mistake was to use equation 2.5 when the circuit was working in a linear scale, instead of using the linear approach (see Table 2.1). The result is shown in the last graph, where only the extremes of the function are equalized. The middle-points are amplified reaching the maximum difference of 5dB in the centre of the input power range (see Fig 2.4b).

Table 2.1: Linear approach and logarithmic approach for equalization

	Linear Approach	Logarithmic Approach
Gain function	$\frac{P_{min}}{P_{in}} \cdot G_{max}$	$(-P_{in_{dB}} + P_{min_{dB}}) + G_{max_{dB}}$
Function	Non-linear	Linear

To sum up, in this section two different approaches are demonstrated. Logarithmic approach shows a linear function respect to the input power to equalize the packets. Linear approach denotes a function where the input power is non-linear since we are not working in logarithmic scale. That bug was found out when the prototype was in the characterisation stage. In the next chapters are shown how that fault is fixed by adding an intermediate log-stage.



(a) Equalization fundamentals on linear range

(b) Absolute error between the ideal equalization and the wrong approach

Figure 2.4: Linear approximation

2.2 Circuit design

In this section, the stages of the analog design are introduced:

- Stage 1: Transimpedance amplifier: current-to-voltage circuit.
- Stage 2 : DC-coupled log amplifier: linear-in-dB circuit
- Stage 3: Scaling amplifier: adapting circuit
- Stage 4: Voltage-controlled current source: voltage-to-current circuit.

In Figure 2.5 the four stages are depicted, where the transimpedance stage converts the optical input power into output voltage. Then, logarithmic amplifier linearises the voltage in front a dB scale. Followed by the scaling amplifier, where it adapts the output voltage of the logarithmic stage to the necessary one to the last stage. Finally, the voltage-controlled converts againg the voltage into current, feeding the proper SOA bias current for equalization.

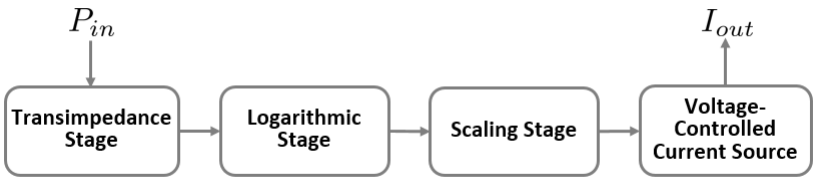


Figure 2.5: Stages of the analog circuit

Before explaining each stage in detail, a brief introduction about the key aspects is explained covering the analog design considerations in [15].

2.2.1 Stage 1: Transimpedance circuit

Transimpedance amplifier is typically used as current-to-voltage circuit for optical receivers. A low input impedance allows to convert the input current into a voltage preserving a high bandwidth.

The main specifications are sensitivity, speed and transimpedance gain. The designer have to achieve a trade-off between those specifications in the design stage. Equation 2.13 shows the output voltage as follows:

$$V_{OUT} = -R_F \cdot I_{PD} \qquad \text{where} \qquad I_{PD} = R_{PD} \cdot P_{IN} \tag{2.13}$$

where R_F is the feedback resistor, I_{PD} the photodiode current, R_{PD} the responsivity in (A/W) and P_{IN} the input optical power. Normally, the generator is a photodiode, whose role is to convert the photons to electrons. Then, the current is amplified by the feedback resistor. As a first approximation, all the signal that comes from the photodiode is transmitted to the output, no bias offset current is present. The output is low impedance, so accepting different loads to be connected. The bandwidth of the circuit is a function of the input capacitance and the gain bandwidth product of the amplifier. Finally, the stability is an important aspect to take into account, it determines the response and the reliability in front the whole frequency spectrum.

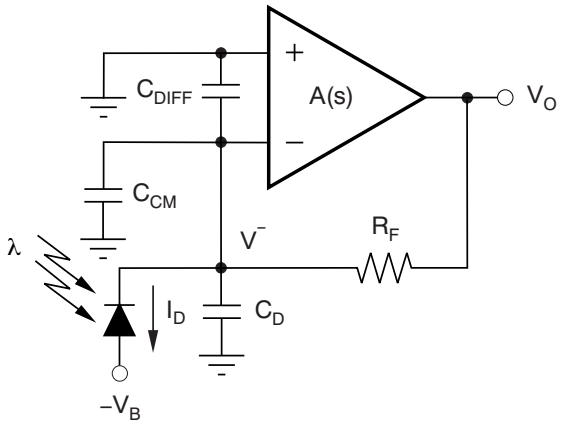


Figure 2.6: Transimpedance amplifier schema

Figure 2.6 shows a transimpedance amplifier modelled with elements. The differential capacitor (C_{DIFF}) and common mode capacitor (C_{CM}) are in parallel with the junction capacitor of the diode. Hence, the total input capacitance is the sum of the amplifier capacitance and the diode capacitance. This will determine the bandwidth of the circuit. For our application, an exhaustive stability analysis is carried out to reach the slew rate and distortion performance. Using a simplified model for the photodiode, the feedback factor is a RC filter with the combination of the feedback resistor and the total input capacitance.

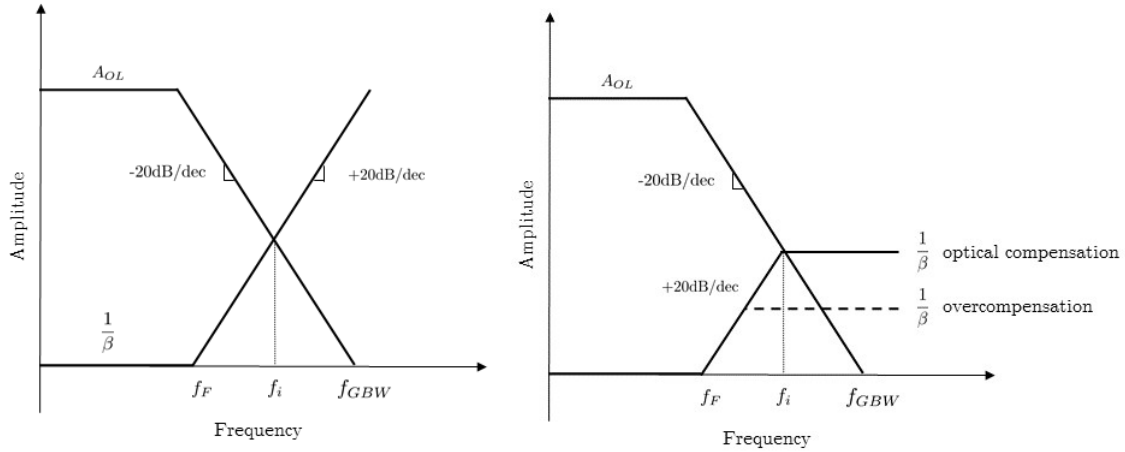
$$\beta = \frac{Z_{C_T}}{R_F + Z_{C_T}} = \frac{1}{1 + j\omega R_F C_T} \tag{2.14}$$

The inverse of the feedback factor is, also called noise gain :

$$\frac{1}{\beta} = 1 + j\omega R_F C_T \tag{2.15}$$

The intersection of the A_{OL} response with the inverse of the feedback factor denotes a critical intercept for the stability analysis (see Figure 2.7a). The ratio of closure at this intersection determines an approximation of the phase margin. The circuit is unstable if the two response curves have a 40dB/dec of ratio of closure.

The compensation consists on providing the optimal phase shift to the intersection point has a ratio of closure of 20dB/dec and the phase margin increases to a higher values. The easiest way to compensate is by adding a bypass capacitor in parallel with the feedback resistance (see Figure 2.7b).



(a) Magnitude plot, open-loop gain and noise gain against the frequency response

(b) Addition of a bypass capacitance affects the magnitude response of the feedback factor

Figure 2.7: Stability criterion graphics

The feedback factor is recalculated taking into account that capacitance:

$$\beta = \frac{Z_{C_T}}{R_F || Z_{C_F} + Z_{C_T}} = \frac{1 + j\omega R_F C_F}{1 + j\omega R_F (C_T + C_F)} \tag{2.16}$$

The noise gain is:

$$\frac{1}{\beta} = \frac{1 + j\omega R_F (C_T + C_F)}{1 + j\omega R_F C_F} \tag{2.17}$$

From equation 2.17, we can difference two noise gains: low-frequency noise gain and high frequency noise gain:

$$\frac{1}{\beta} = \left.\frac{1 + j\omega R_F (C_T + C_F)}{1 + j\omega R_F C_F}\right|_{\omega=0} = 1 \qquad \text{(low-frequency noise gain)} \tag{2.18}$$

$$\frac{1}{\beta} = \left.\frac{1 + j\omega R_F (C_T + C_F)}{1 + j\omega R_F C_F}\right|_{\omega=\text{inf}} = 1 + \frac{C_F}{C_G} \qquad \text{(high-frequency noise gain)} \tag{2.19}$$

A large bypass capacitance adds a zero in the feedback factor, also modifies the position of the pole. That zero compensates the phase shift introduced by the pole reducing the ratio of closure to 20dB/dec, and this overcompensation also reduces the bandwidth of the transimpedance amplifier. An optimum value of the capacitance is necessary to achieve the best performance of the amplifier, where the zero is located at the interception of the open loop gain and the inverse of the feedback factor, in other words, to target 45 degrees of phase margin. From equation 2.16 the feedback pole and feedback zero are located :

$$f_F = \frac{1}{2\pi R_F (C_T + C_F)} \tag{2.20}$$

$$f_i = \frac{1}{2\pi R_F C_F} \tag{2.21}$$

From Figure 2.7a one can solve graphically the intersection point related with the new zero since both slope are the same and an isosceles triangle is formed.

$$\log(f_i) = \frac{\log(f_F) + \log(f_{GBW})}{2} \tag{2.22}$$

Rewritting the equation without log:

$$f_i = \sqrt{f_F \cdot f_{GBW}} \tag{2.23}$$

Once we have the relation of the intersection frequency with the unity-gain frequency, and the pole of the feedback factor, the value of the bypass capacitance is obtained :

From equations 2.20, 2.21 and 2.23 we acquire:

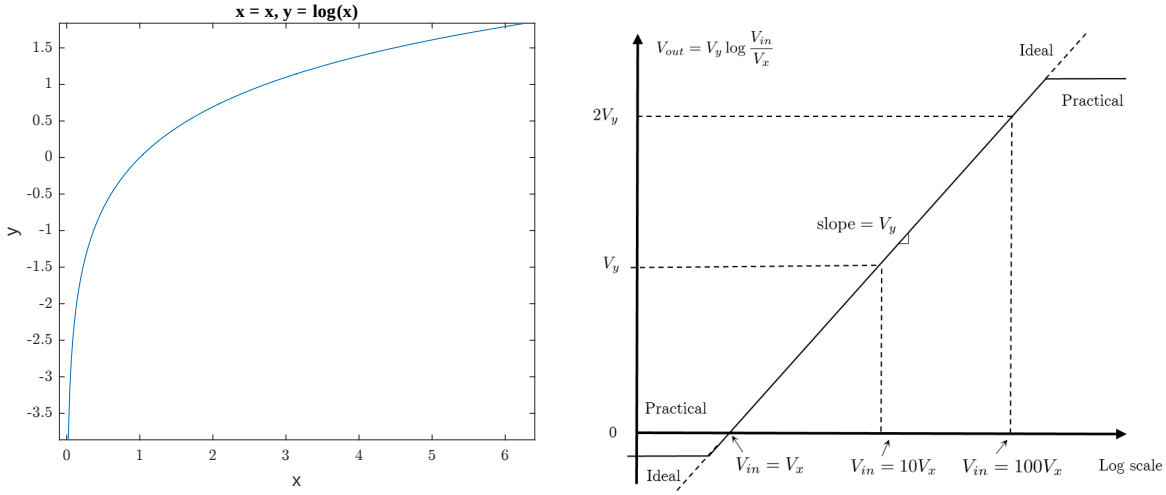
$$\left(\frac{1}{2\pi R_F C_F}\right)^2 = \frac{f_{GBW}}{2\pi R_F (C_T + C_F)} \tag{2.24}$$

This leads us to a conventional quadratic equation:

$$C_F = \frac{1}{4\pi R_F f_{GBW}}(1 + \sqrt{1 + 8\pi R_F C_T f_{GBW}}) \tag{2.25}$$

2.2.2 Stage 2: Logarithmic amplifier

A logarithmic amplifier is an operational amplifier that convert a signal to a its logarithmic value, normally it encloses a non-linear operation. Before explaining a typical log amp transfer function is necessary to fully understand a log function. Thus if $\log(x) = X_1$, a $\log(x \cdot y) = X_1 + Y_1$, $log(x^2 \cdot y) = 2X_1 + Y_1$ and $\log(x/y) = X_1 - Y_1$.



(a) log function

(b) Practical plot of log response

Figure 2.8: Logarithmic function, ideal and practical

Figure 2.8a depicts a log function, where y tend to minus infinity as x approaches to zero, and where y is zero when x is unity. In a practical log amplifier the transfer function follows the next equation:

$$V_{OUT} = V_Y \log \frac{V_{in}}{V_x} \tag{2.26}$$

V_Y is the slope voltage units, the logarithm is usually taken to base 10, volts-per-decade. The intercept is the point at which the linear response or the extrapolated one intersect the horizontal axis ($V_{in} = V_x$). So, one can say that the transfer function of a log amplifier is driven by the slope and the intercept. The accuracy of those scaling voltage also sets the absolute accuracy of the logarithmic amplifier.

On the contrary of the ideal log function, when the inputs are very close to zero, log amps starts to saturate. This is usually for the noise of the device, then it often limits the dynamic range of a log amp (see Figure 2.8b). Precise control of the slope and intercept results in a log amp with stable scaling parameters, making it a true measurement device.

There are two most-used architectures which are used to acquire a log response: basic diode/transistor log amp and successive detection log amp. In a diode base log amp, a diode is placed in the feedback path of an inverting op-amp, then the output voltage is proportional to the logarithm of the input current, since the voltage across a diode is proportional to the logarithm of the current that flows through it.

So, the dynamic range is limited by the non-linearities of the diode (around 40 to 60 dB), but by using a transistor-diode based, the dynamic range can be extended to 120dB or more. The main drawbacks of that first of architecture are: temperature dependence, positive input signals, and its bandwidth is both dependent and limited on the signal amplitude. This last drawback is the major disadvantage since however precisely is the amplifier designed, there will be always a residual feedback capacitance from the output to input. That capacitance, known as Miller capacitance, generate a time constant with the impedance of the emitter-base junction, in such a manner that a low-pass corner frequency is appeared.

$$f_{3dB} = \frac{1}{2\pi r_{eb} C_c} \quad \text{where} \quad r_{eb} = \frac{1}{g_m} = \frac{kT}{qI_C} \tag{2.27}$$

The resistance of the emitter-base junction is inversely proportional to the current flowing in it, so the equation 2.28 shows the proportionality of bandwidth to current, where q is the electron charge, k is the boltzmann constant and T the temperature .

$$f_{3dB} = \frac{qI_c}{2\pi kTC_c} \tag{2.28}$$

To summarize, it is very hard to develop a log amp with that architecture with a bandwidth greater than few hundred KHz.

Moving towards the second architecture, successive detection log amplifiers, the natural-logarithmic law of the diode is substituted by a new design that uses a number of similar cascaded stages having well-defined large signal behaviour.

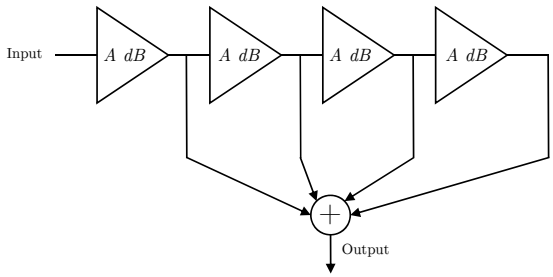


Figure 2.9: Basic successive log amp architecture

Figure 2.9 depicts a N cascaded limiting stages where the output of each stage is fed to a summing circuit. If the input signal is small enough, the output is controlled by the last stage $G = N \cdot A\ dB$. As the input signal is increasing, the last stage saturates and limits the signal. So, it does not add more gain, the total gain drops to the previous stage (N-1)A dB. As the input signal continues increasing, the incremental gain drops to (N-2)A dBm and so on until the output saturates (see Figure 2.10). This is an ideal and very general model to demonstrate the principle, but its implementation at very high frequencies is challenging. The delay between the different paths becomes problem in some systems, the solutions of these mismatches are not explained in this thesis because it is not an interested topic. All in all, this second architecture allows us to achieve a fast response time since the limitation is now on the architecture of the successive amplifiers. In the next chapter, the topology of the circuit is simulated and explained.

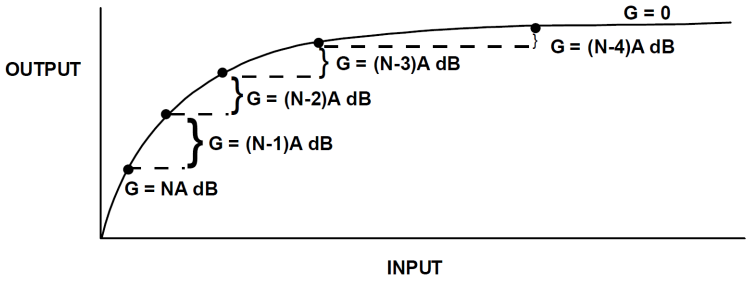


Figure 2.10: Basic successive log amp response

2.2.3 Stage 3: Scaling Amplifier

This stage is intended to re-scale the output voltage of the logarithmic amplifier to a range of input voltage of the SOA drivers. The circuit consists on an inverting topology with a reference voltage, where the slope is determined by the ratio of resistances and the reference voltage by the potentiometer. Changing the slope and the reference voltage the equalizer can provide different output for the same optical power, so depending on the transfer function of the SOA, the ratio of resistances and the potentiometer must be consequently dimensioned .

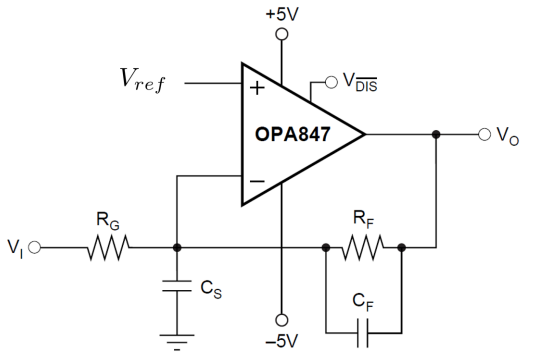


Figure 2.11: Scaling amplifier: inverting configuration with reference voltage

The output voltage of the circuits follows :

$$V_{OUT} = -\frac{R_F}{R_G}V_{IN} + \left(\frac{R_F}{R_G} + 1\right)V_{REF} \tag{2.29}$$

Just introducing the structure of the operational amplifier that is used, bipolar technology is characterized by a high bias current. That current has to be reckoned in order to calculate correctly the offset, then the formula stays as:

$$V_{OUT} = -\frac{R_F}{R_G}V_{IN} + \left(\frac{R_F}{R_G} + 1\right)V_{REF} - I_b R_F \tag{2.30}$$

The reference voltage is affected by the ratio of the resistance as well as the input bias current is affected by the feedback resistance. It means that if the feedback resistance is enough high the bias current will start to be significant to such an extent that the output voltage of the circuit is highly modified.

Moving towards the stability of the circuit, the procedure is the same to the previous. That external compensation technique can be used to retain the full slew rate of the operational amplifier. Recalling the Figure 2.7, the inverse of the feedback factor ($\frac{1}{\beta}$) can be defined as low-frequency noise gain (N_{G1}) and as high-frequency noise gain (N_{G2}).

$$N_{G1} = 1 + \frac{R_F}{R_G} \tag{2.31}$$

$$N_{G2} = 1 + \frac{C_S}{C_F} \tag{2.32}$$

The ratio of the capacitance set both the transition frequencies and the high-frequency noise gain. If that noise gain (N_{G2}) is set to a value greater than the recommended minimum stable gain for the operational amplifier, and the pole placed correctly (see equation 2.20), a very flat response can be achieved.

In order to choose the values for both capacitances, two variables and three equations need to be solved. The first variable is to fix the high-frequency noise gain greater than the minimum stable gain. The second variable is also set the low-frequency noise gain, where for our application, the ratio of resistances scale the signal from 1 up to 2.

$$N_{G1} = 1 + \frac{R_F}{R_G} = (1+1)||(1+2) \tag{2.33}$$

$$N_{G2} = 1 + \frac{C_S}{C_F} = G_{min} \approx 20 \tag{2.34}$$

So, using only those two gains and the GBP for the op amp, the key frequency in the compensation is:

$$f_F = \frac{GPB}{NG_1^2}\left[\left(1 - \frac{NG_1}{NG_2}\right) - \sqrt{1 - 2\frac{NG_1}{NG_2}}\right] \tag{2.35}$$

Physically, f_F is the feedback pole that is set by equation 2.21. The feedback zero in the noise gain occurs at $N_{G1} \cdot f_F$ and the feedback pole in the noise gain occurs $N_{G2} \cdot f_F$. Then, that pole is set by $1/R_F C_F$, C_F can be obtained as follows:

$$C_F = \frac{1}{2\pi R_F f_F N G_2} \tag{2.36}$$

By using equation 2.32, one can determine C_S:

$$C_S = (NG_2 - 1)C_F \tag{2.37}$$

Finally, the maximum bandwidth will be achieved for a butterworth response with Q = 0.707. This result is an interesting point because this is also equivalent to saying that the 3dB bandwidth is equal to f_i:

$$f_{-3dB} = \sqrt{f_F f_{GBP}} \tag{2.38}$$

2.2.4 Stage 4: SOA driver

Figure 2.12 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in accordance with the sign and magnitude of the control voltage. The input signal applied in the first amplifier, appears at the negative input if the feedback loop is decently closed. In the steady state, the signal comes along the output of the second amplifier A2, which is a fix-gain amplifier 20dB, and it is applied across the sense resistor with a reduction of 1/10. Then, the output current is merely:

$$I_{OUT} = \frac{V_{IN}}{R_{sense} \cdot 10} \tag{2.39}$$

Regarding the stability of the circuit, the compensation capacitance within the output resistance of the second amplifier forms a dominate pole for the loop, while the feedback amplifier is fast enough to be transparent in the path. The ratio of the load resistor to the sense resistor has to be approximately 10:1 or greater for a straightforward compensation.

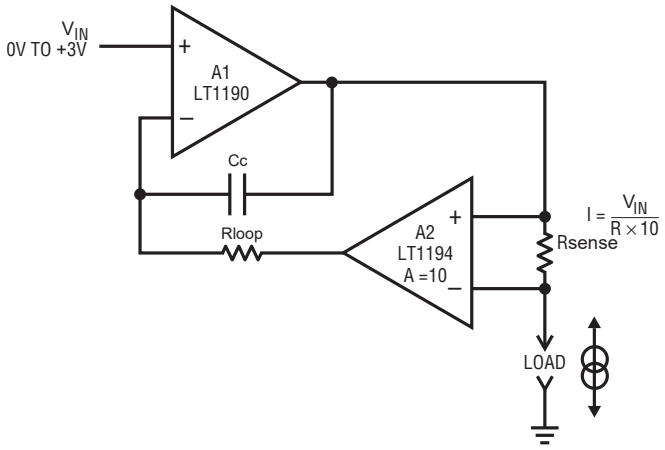


Figure 2.12: Voltage Controlled Current Source with Grounded Load

2.3 Design equations

In this section, a global analysis of the system is introduced. The goal is to obtain the correct values for the scaling stage in terms of slope and reference voltage. Table 2.2 illustrates the corresponding equations of each stage. Since the transfer function of the SOA determines the behaviour of the circuit, the flow-design comes from the last stage up to the first one.

Table 2.2: Equations for each stage

	Output response
Stage 1	$V_{OUT_{TIA}} = R_F R_{PD} P_{IN}$
Stage 2	$V_{OUT_{LOG}} = V_y \log\left(\frac{V_{OUT_{TIA}}}{V_x}\right)$
Stage 3	$V_{OUT_{SCA}} = -\frac{R_F}{R_G} V_{OUT_{LOG}} + \left(\frac{R_F}{R_G} + 1\right) V_{REF} - I_b R_F$
Stage 4	$I_{OUT} = \frac{V_{OUT_{SCA}}}{10 R_{sense}}$

From the one hand, equations 2.40, 2.41 come from the voltage-controlled current source, the sense resistor and maximum/minimum output current fix the values of the input voltage of the voltage controlled current source. Thus, those input voltage values have to match within the incoming optical power.

$$V_{max_{\text{stage4}}} = 10 R_{sense} I_{max} \tag{2.40}$$

$$V_{max_{\text{stage4}}} = 10 R_{sense} I_{min} \tag{2.41}$$

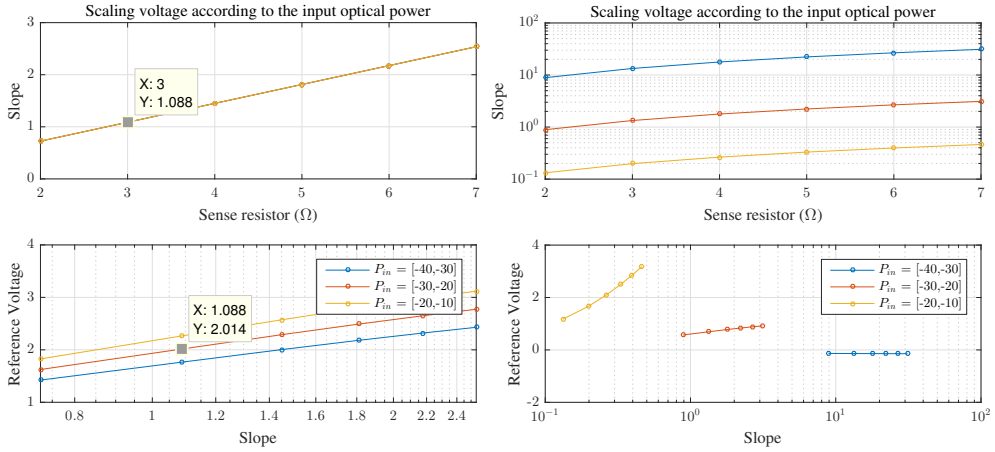
From the other hand, equations 2.42, 2.43 refers to the output voltage of the log-amplifier equivalent to the maximum and minimum values of the optical power.

$$V_{max_{\text{stage2}}} = V_y \log\left(\frac{V_{max_{(\text{stage1})}}}{V_x}\right) \tag{2.42}$$

$$V_{min_{\text{stage2}}} = V_y \log\left(\frac{V_{min_{(\text{stage1})}}}{V_x}\right) \tag{2.43}$$

$$\tag{2.44}$$

So, the slope of the scaling amplifier is calculated following the next equation:



(a) Log-approximation (b) Linear-approximation

Figure 2.13: Design criterion graphs, slope and reference voltage determined by the input optical power and the sense resistor of the last stage

$$\text{slope} = \frac{R_F}{R_G} = \frac{V_{max_{\text{stage4}}} - V_{min_{\text{stage4}}}}{V_{max_{\text{stage2}}} - V_{min_{\text{stage2}}}} \tag{2.45}$$

Once the slope is fixed, the reference voltage is estimated substituting $V_{in} \rightarrow V_{max_{\text{stage2}}}$ and $V_{OUT} \rightarrow V_{max_{\text{stage4}}}$. Equation 2.46 shows the reference voltage in function of the slope, the input voltage and the output voltage.

$$V_{REF} = \frac{slope}{1 + slope}(+I_b R_G + V_{max_{\text{stage2}}}) + \frac{1}{1 + slope} V_{max_{\text{stage4}}} \tag{2.46}$$

By using the previous equations, one can obtain an approximation of the required value for the scaling amplifier stage. This approach have to be tuned afterwards once the experimental setup is set. Moreover, Figure 2.13a shows a graphical representation of those values, making the calculations easier.

Two important facts can be highlighted. Since the log-amplifier stage linearises the output voltage respect to the input optical power in dBm, the slope is the same independently of the range of it. On the contrary, the circuit design without the log-stage has highly dependency on the incoming optical power range, making more difficult a right equalization between two points (see Fig 2.13b). The other fact to point out is the reference voltage, where it is clear that the lower the optical power range, the higher has to be the reference voltage to keep the same values for the last stage.

2.4 Summary

In this chapter, the mathematical concept of equalization, specification of a feasible system and circuit design have been presented. Analysing two approaches of equalization, logarithmic and linear, indicate that the solution is to go for the logarithmic approximation. Hence, the output response follows a linear relationship with the input power in dB, allowing a fast analog circuit design. In addition, the slope of the scaling amplifier is totally independent of the input optical power range, thus only the reference voltage is affected by that variable. Circuit design section has shown the main points of each stage, including the biasing and stability analysis. Finally, a preliminary calculation for both approaches has been reported, where the values are used as starting point for the simulations.

Chapter 3

Simulation and components selection

In this Chapter, a full simulation is performed to verify that theoretical design can be implemented with the proper components. A powerful SPICE simulator -*LTSPICE*- schematic capture and waveform viewer allows us to make extremely fast simulations by using macro models of the practical components and including all non-linearities of the devices.

The three main simulation modes used for the design are:

1. **DC Analysis**: Simulation to set the operation point of the circuit. It determines voltage range and consumption of the components. On DC Analysis, only Ohm's Law is applied, with inductors shorted and capacitors opened.

2. **AC Analysis**: Small-signal analysis calculates AC output variables as a function of frequency. The program first computes the DC operating point of the circuit and determines linearised, small-signal models for all the non-linear devices in the circuit. The stability of the circuit is determined by this analysis.

3. **Transient Analysis**: The transient analysis computes the output variables as a function of time over a user-specified time interval. This analysis shows the response time of the circuit in front an input step. Two measurements are distinguished along this thesis: rising time and settling time. The rise time is defined as the time required for the response to rise from 10% to 90% of its final value. For the settling time, it is defined as the time elapsed from a step input to the time at which the output has entered and remained within a specified error band, in our case, 1% error band.

In the following, section 3.1 introduces the schematic used to simulate the first stage of the circuit. In section 3.2, log stage is composed by two sub-stages in order to achieve the best response time. Section 3.4 presents the simulation of the scaling amplifier, where two prototypes are discussed and explained. A detailed analysis of the stability issue is introduced for each configuration. The last stage is studied by exploiting all the possibilities in terms of biasing and time in section 3.5. Finally, the overall behaviour is demonstrated by simulating the full design -steady state, response time and power consumption in section 3.6.

3.1 Transimpedance Amplifier

For the next two stages a wideband, ultra-low noise, voltage-feedback operational amplifier is presented. Texas Instrument OPA847 combines very high gain bandwidth and large signal performance with an ultra-low input noise voltage (0.85nV/Hz) while using only 18mA supply current [16]. The OPA847 also includes an optional power shut-down pin that, when pulled low, disables

the amplifier and decreases the supply current to 1% of the powered-up value. For prototyping is not used, but it is interesting for a future outlooks.

The combination of very low input voltage and current noise, along with a 3.9GHz gain bandwidth product, make the OPA847 an ideal amplifier for wideband transimpedance applications. Moreover, a high slew rate of 950V/μs provides it a fast response time.

The current generated by the photodiode is replaced by an ideal current source at the input of the amplifier. Including the same resistance to ground on the non-inverting input, the output DC error is minimized (see Figure 3.1). In parallel, 100pF and 10pF are included to minimize the output noise contribution of this resistor.

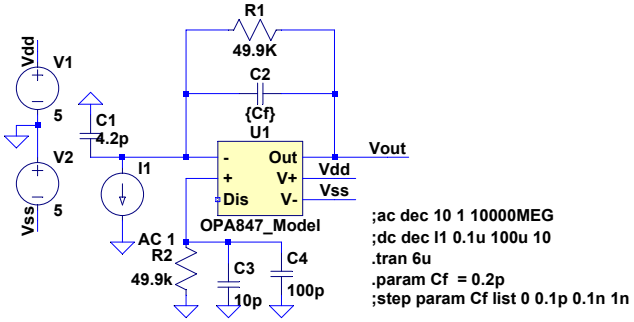


Figure 3.1: Schematic of the transimpedance amplifier

3.1.1 DC Analysis

This first analysis consists in checking the output response of the transimpedance amplifier. Parametric sweep of the transresistance gain is performed to observe the sensitivity of the circuit and the saturation point. Since the PSPICE simulator can not emulate a laser and a photodiode, we have to suppose the responsivity of it and use directly a current source as it is said before. The input current goes from 1μA up to 1mA, so that corresponds to an input optical power from -30dBm up to 0 dBm. Figure 3.2 shows the output voltage depending on the feedback resistance.

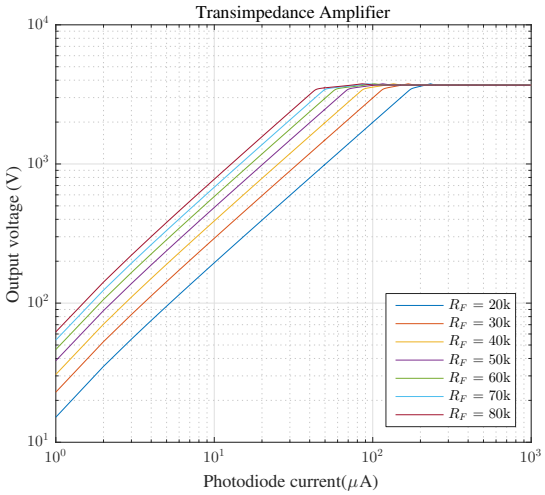


Figure 3.2: Parametric sweep of the transimpedance gain from $R_F = 20k\Omega$ up to $R_F = 80k\Omega$

3.1.2 AC Analysis

In the previous chapter we introduced some terms such as loop gain, closed/open-loop gain or feedback factor. In this section the stability of the circuit is analysed according to what was explained in the chapter 2. The rate of closure or the phase margin measurements can not be acquired from the standard closed-loop schematic. Figure 3.3 represents the specific configuration for an AC Analysis. The feedback loop of the circuit is opened up, the AC source excite the high-impedance side where the feedback loop is split.

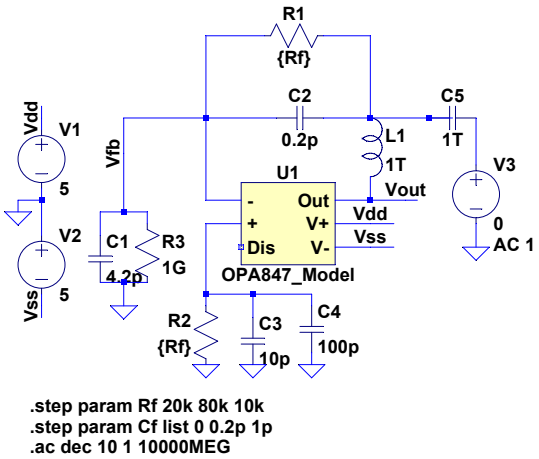


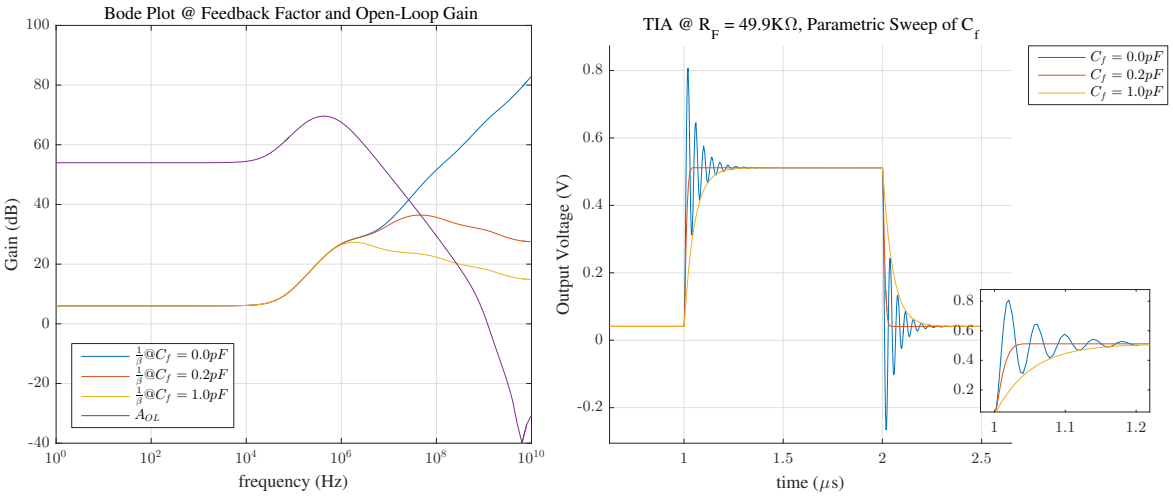
Figure 3.3: Schematic of the transimpedance amplifier for AC analysis

Nonetheless, the circuit needs to be properly biased otherwise the output saturates to the power supply voltage. To do so, the circuit must emulate a closed loop feedback at DC frequency and open loop for all AC frequencies. By using an inductor and a capacitance with high values, the result is exactly what we want. At DC, the inductor is a short-circuit meanwhile the capacitance is an open-circuit. For AC, it is the other way around, resulting then in the proper configuration. Once the DC point is verified, a AC transfer characteristic analysis over the operational amplifier bandwidth is performed. Bode plot shows the frequency response of the system, where the magnitude is expressed in dBs. Figure 3.4 shows two methods to measure indirectly the phase margin of the circuit. By analysing the rate of closure of the open-loop gain and the noise gain at its intersection point, one can quickly determine the stability of the circuit. Figure 3.4a shows three different cases where the feedback capacitance determines the slope of the noise gain.

In the first case, where the circuit has not feedback capacitance, we have a rate of closure of 40dB/decade. It causes instability in the circuit, as it is depicted in the Figure 3.4b. There is a zero well before the unity-gain frequency, which makes $1/\beta$ increase with a slope of 20dB/decade.

In the second case, the feedback capacitance takes a value of 200fF, the value is a bit higher than the calculated with the formula 2.25 ($C_F = 60fF$) the maximum flat-response is obtained with that value. At the intersection frequency, the noise gain has a flat-shaped response having then a rate of closure of 20dB/dec. The phase margin corresponds between 45 and 90 degrees.

In the final case, an over-dimensioned feedback capacitance is chosen. The time response shows a rising time quite longer than the optimal value. The circuit is still stable, but if we keep increasing the value of the capacitance, the addition pole would make the response unstable since the intersection between both would be in a slope of -40dB/dec.

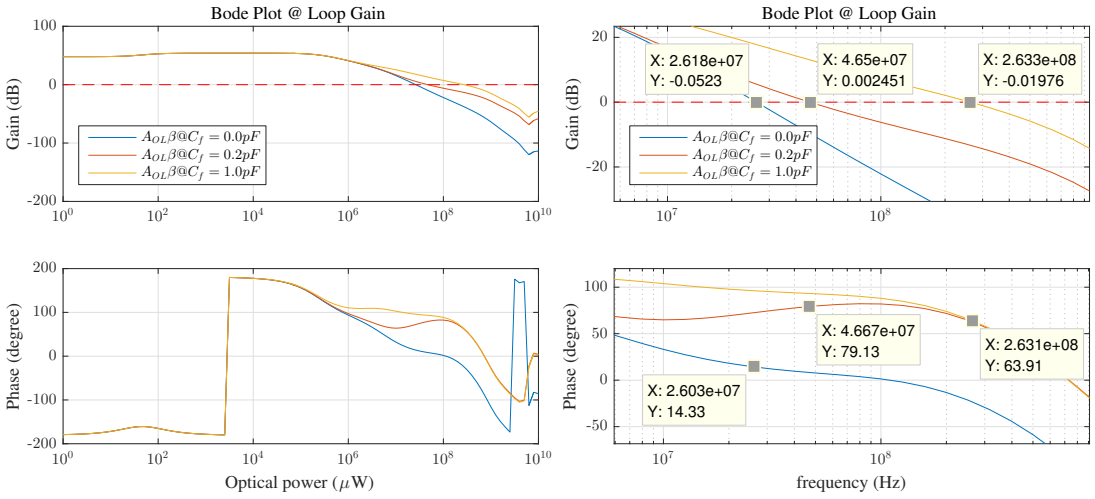


(a) Magnitude Bode plot of open-loop gain and noise gain, parametric sweep of the feedback capacitance

(b) Output response in front of input step

Figure 3.4: Indirect methods for stability analysis

Figure 3.5 represents the phase margin measurement. The magnitude and phase of the loop gain are plot in order to evaluate the phase at which the magnitude is 0 dB. Focusing on the Figure 3.5b we observed that the circuit without any compensation has a phase margin of 14.33 degrees, indicating an unstable condition. For the optimal case, the phase margin achieves 79.13 degrees, ensuring zero overshooting. Finally, the last case occurs with a phase margin of 64 degrees.



(a) Bode plot -Magnitude and phase- of loop gain, phase margin measurement

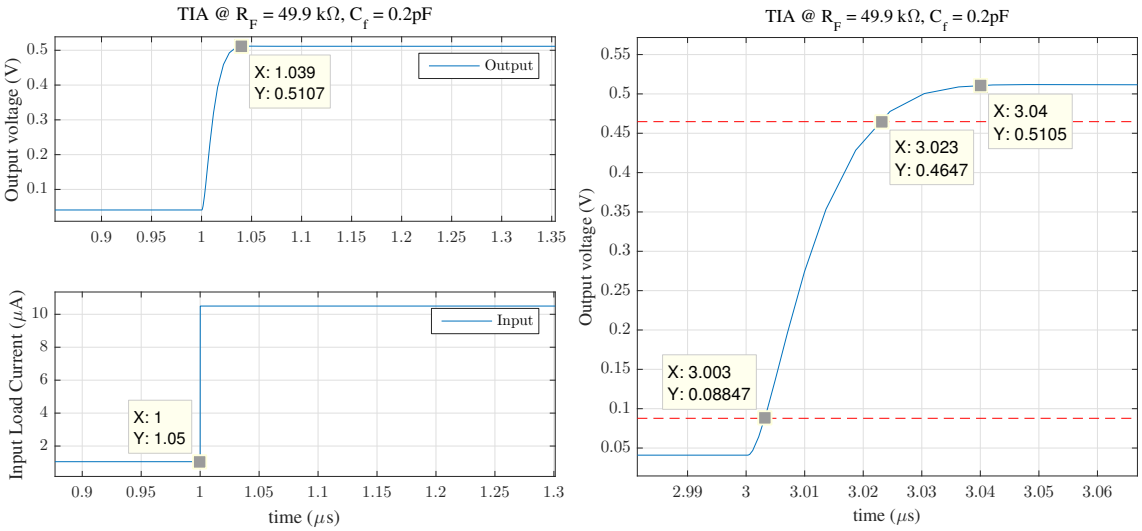
(b) Zoon-in where the loop gain reaches 0 dB gain, phase margin measurement

Figure 3.5: Phase margin calculation

3.1.3 Transient Analysis

After a full stability analysis, the response time is calculated with the values chosen before. The rising time is 20 ns at the output of the transimpedance amplifier. For the settling time, a total

of 40 ns is measured. That time is a good starting since our application requires less than 100 ns (see Figure 3.6a).



(a) Response time of the circuit, input current from $1\mu A$ up to $10\mu A$

(b) Measuring rising time/settling time

Figure 3.6: Transient analysis - TIA

3.2 Logarithmic Amplifier

For this stage, a logarithmic amplifier with a very fast voltage mode output is selected. It uses the progressive compression technique (successive detection) to provide a dynamic range of up to 95 dB and a rise time of 15 ns . Normally, multistage demodulating logarithmic amplifiers are used to provide a baseband video response or accept an RF input and demodulate this signal to develop an output that is essentially the envelope of the input represented on a logarithmic or decibel scale. In our case, the component selected is AD8310. This IC provides the possibility to operate in DC-coupled input. There is no minimum frequency limit; the AD8310 can be used down to low audio frequencies, even DC [17].

A fully differential input is essential, however, our source is a single-sided ground-referenced signal. Besides, its differential inputs must be positioned at least 2 V above the COM potential for proper biasing of the first stage. Hence, a level-shifting and a single ended to differential conversion is required. For the single-ended input to differential output, AD8138 is the best candidate because of its fast response and easy common-mode level-shifting configuration [18].

Figure 3.7 shows the two ICs that conform the logarithmic stage. The AD8138 is configured for unity gain for a single-ended input to differential output by means of the four 499 Ω resistors. The level-shift is achieved by applying 2.5V from the resistive divider referenced to the power-supply.

Another aspect to highlight is the offset voltage of the logarithmic amplifier. In this application, the offset compensation is done by grounding the circuits input and slightly varying the gain resistors on the inverting input of the AD8138 until the voltage on the AD8310's output reaches a minimum. To do so, the internal offset compensation is disabled by applying a voltage of 1.9V approximately and adding a potentiometer to the negative input of the first amplifier (R_{off} in the schematic).

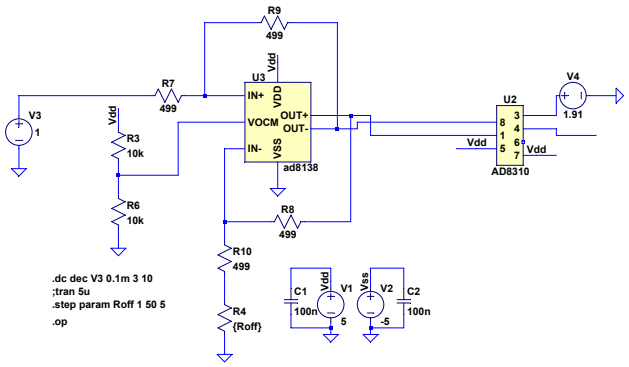


Figure 3.7: Schematic of the logarithmic stage

3.2.1 DC Analysis

In this section, the steady-state behaviour is presented. To show how sensitive is the log-stage to the symmetry of the system a parametric sweep is performed. Figure 3.8 shows how an unbalanced input signal affects to the output voltage. Being a simulation, both paths are symmetrical and the offset compensation is obtained when the potentiometer achieves a value of $R_{\text{off}} = 1\Omega$, only an increment of 5Ω has a dramatical consequence, losing linearity and dynamic range at the output. For the practical stage, the offset compensation is more than necessary since the parasitic from the board, resistances and pins will affect to the system.

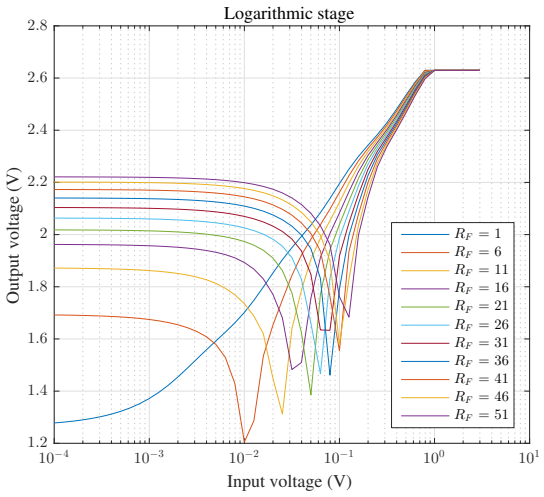


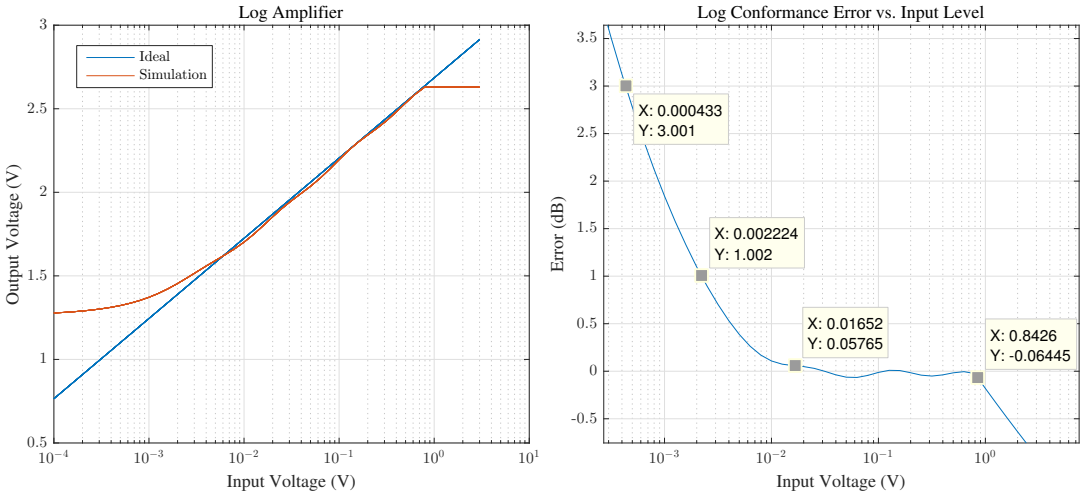
Figure 3.8: Output voltage response sweeping the offset resistance.

Concerning the output and input voltages (for $R_{\text{off}} = 1\Omega$), the slope is nominally 480mV/dec. Therefore, two decades change at the input results in a change at the output of approximately 960mV. Log-plot shows the range over which the device maintains its slope constant. The dynamic range of the log amp is defined as the range over which the slope remains within a certain error band,usually $\pm 1dB$ or $\pm 3dB$. In Figure 3.9b, for instance, the $\pm 1dB$ dynamic range is from $2.22mV$ up to 3V.

The intercept is the point at which the extrapolated linear response would intersect the horizontal axis . For the AD8310, it is calibrated to be $2.55\mu V$. Using the slope and intercept, the output voltage can be calculated for any input level within the specified input range using the

following equation:

$$V_{out} = V_y \log\left(\frac{V_{in}}{V_x}\right) = \frac{480mV}{dec} \log\left(\frac{V_{in}}{2.55\mu V}\right) \tag{3.1}$$



(a) Ideal response (from equation 3.1) vs simulation (b) Error and dynamic range in $\pm 1dB$ and $\pm 3dB$ error band

Figure 3.9: DC analysis for logarithmic stage

3.3 Transient Analysis

In this section, the response time of the logarithmic amplifier is demonstrated. Figure 3.10 illustrates the response time at the output of stage. An input step of 50mV and 500 mV is simulated to reproduce a real scenario. It shows rise and fall time in an exponential way, which indicates a small signal response.On the one hand, the rising time is 40ns, and as it is said before, the exponential behaviour corresponds to a small signal step. On the other hand, the settling time reaches the final value at 50 ns.

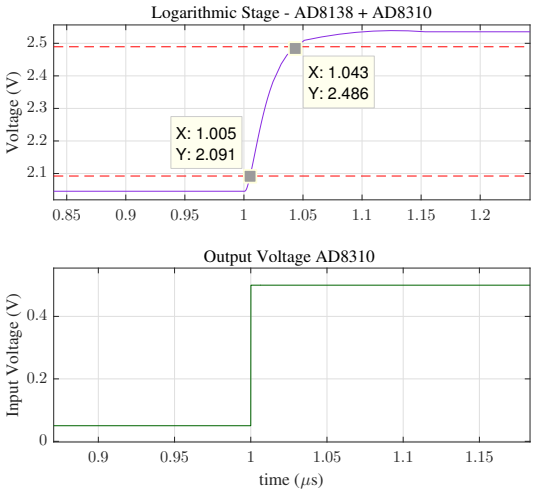


Figure 3.10: Small signal step - 500mV

Figure 3.11 shows the traces of the entire stage, after the unity gain single-ended to differential pair amplifier and the log amplifier. Demonstrating that the critical path is the AD3810 log amplifier.

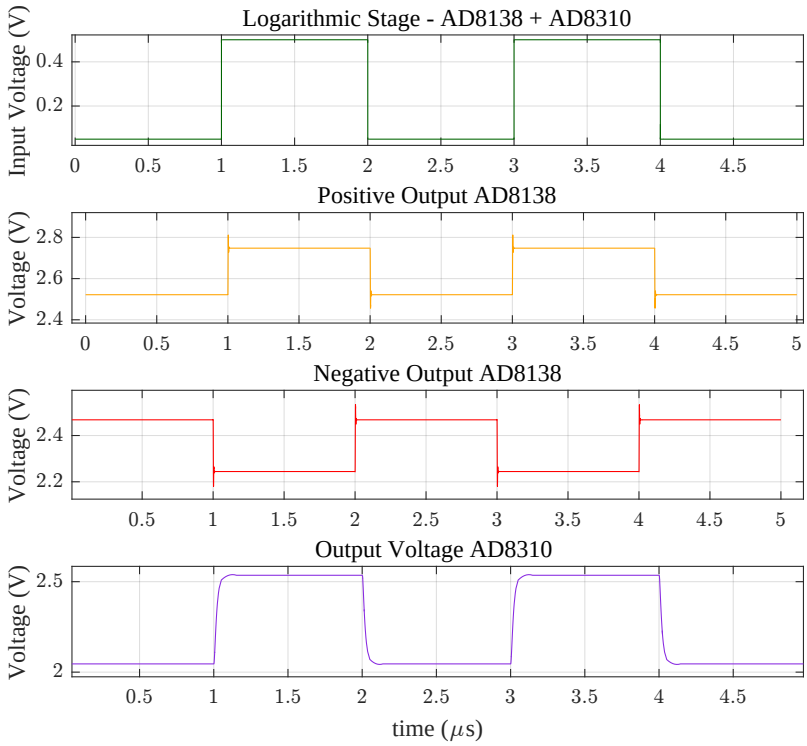


Figure 3.11: Transient Analysis - Response time in AD8138 and AD3810

3.4 Scaling Amplifier

As it is explained in the previous chapter, the purpose of the following stage is to shift the input voltage to a proper range for the SOA driver. Firstly the bias point of the circuit is demonstrated within an exhaustive set of scenarios. Later, a stability and transient analysis are performed to ensure the specifications of the system.

It is important to highlight and clarify some aspects of this stage. The slope and reference voltage are key parameters to fit properly the output current to the transfer function of the SOA. For that reason, two prototypes have been developed. On one hand, a fixed-slope with the ratio of the resistance is designed, in short, the reference voltage is the only variable to play with. On the other hand, full-flexible configuration with variable slope and reference voltage is designed. Both parameters are set by digital potentiometers controlled via I2C protocol.

For the slope, the feedback resistance is substituted by a high-resolution digital potentiometer. AD5272 is 1024-position digital rheostat, with $20k\Omega$ nominal resistance, which ensure less than 1% end-to-end resistor tolerance error.

For the reference voltage, the potentiometer is replaced by another digital potentiometer. AD5259 is 256-position digital potentiometer, with $10k\Omega$ nominal resistance. This device performs the same electronic adjustment function as mechanical potentiometer.

Neither of them has a SPICE model whose can be simulated, so the parasitic capacitance are added manually to the schematic following the data-sheet specifications. In the section 3.4.2 the

stability analysis is performed for both configurations since the values of the resistances dramatically affect to the behaviour of the circuit.

3.4.1 DC Analysis

Figure 3.12 shows the schematic of the scaling stage. The compensation network is set by the ratio of the capacitance C_F and C_G, the slope by R_F and R_G and the reference voltage by a potentiometer (R_α and $R_{(1-\alpha)}$) and a follower circuit. By using that schematic and performing a DC analysis, the results can be observed in the Figure 3.13

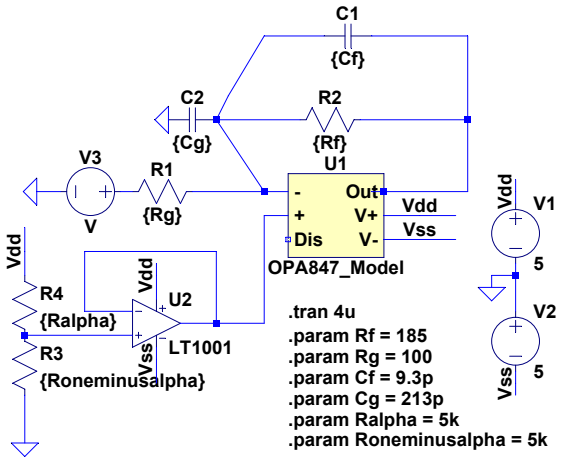
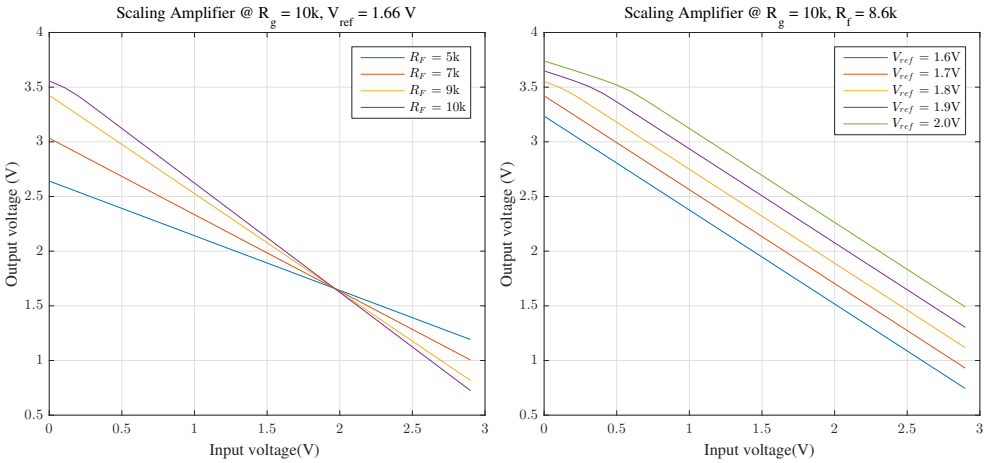


Figure 3.12: Schematic circuit for DC and transient analysis.

Two parametric sweep, one of the feedback resistance and the other of the reference voltage, are introduced in the Figures 3.13a and 3.13b. As it is stated in the equation 2.30, by changing the ratio of the resistances, the slope of the output voltage is modified (see Fig 3.13a). Regarding Figure 3.13b the reference voltage just adjust the offset of the signal, keeping constant the slope. Finally, one can observe that the output voltage start to saturate above 3.5V, it is good news since the working area is lower, around 2.6V down to 1.6V.



(a) DC parametric of feedback resistance

(b) DC parametric of reference voltage

Figure 3.13: DC analysis of Scaling Stage

3.4.2 Stability Analysis

Stability analysis is performed for two different configurations of the scaling amplifier. Recalling the previous chapter, in the section 2.2.3, the stability is presented and discussed. By using those equations, Table 3.1 introduces the starting values :

Table 3.1: Capacitance value for each configuration.

	Full-Flexible $R_F = 8.6k\Omega, R_G = 10k\Omega$	Fixed-slope $R_F = 86\Omega, R_G = 100\Omega$
C_F	19 pF	200fF
C_G	400pF	4.8pF

Once the values of the capacitance are set, AC analysis is accomplished in the same way than Figure 3.14.

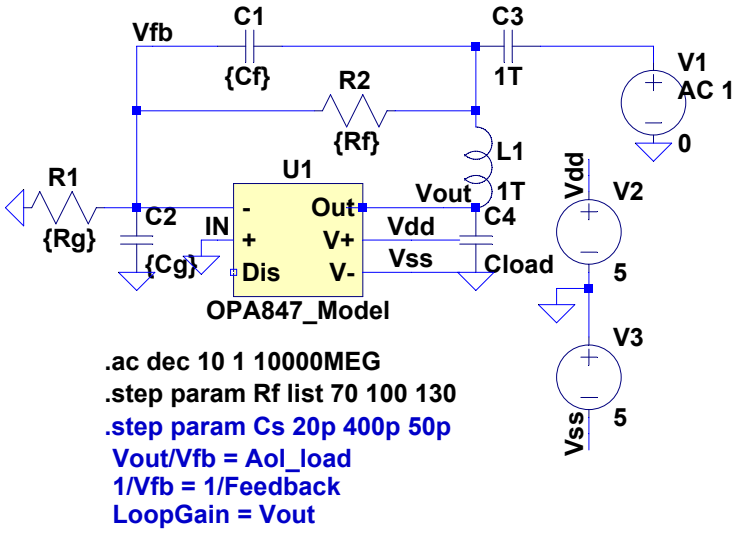
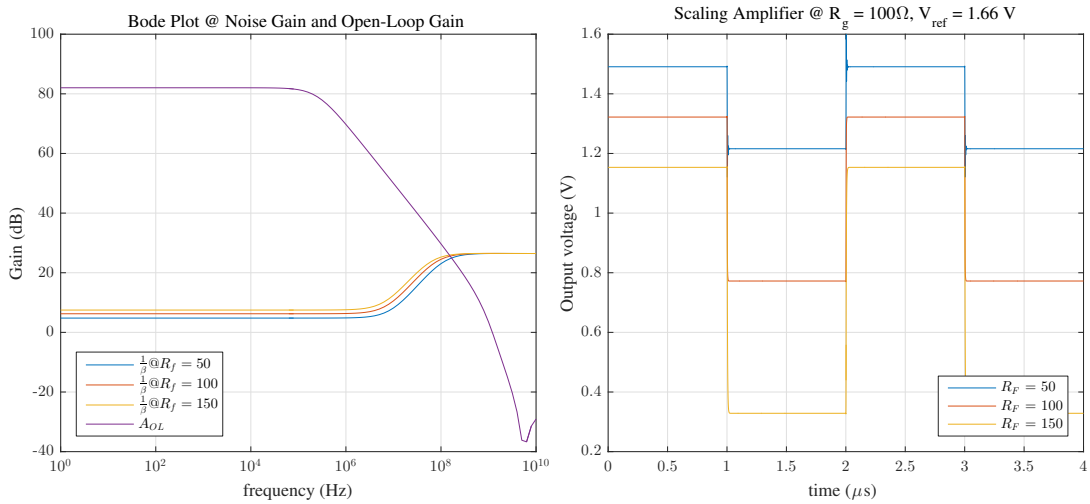


Figure 3.14: Schematic for AC Analysis, fixed-slope and full-flexible

Fixed-Slope

For fixed-slope configuration, where the ratio of resistance can be chosen by any constrain, bode analysis is performed for different slopes keeping the same capacitances. The idea is to observe the phase margin and the stability considering three possible scenarios. Figure 3.15a shows the rate of closure at its intersection point. As a rule of thumb, one can affirm that two out three configurations are stable. Moreover, transient analysis shows that only in the lowest value of the resistance the stability is compromised with a ringing in the beginning of the transient (see Fig 3.15b).

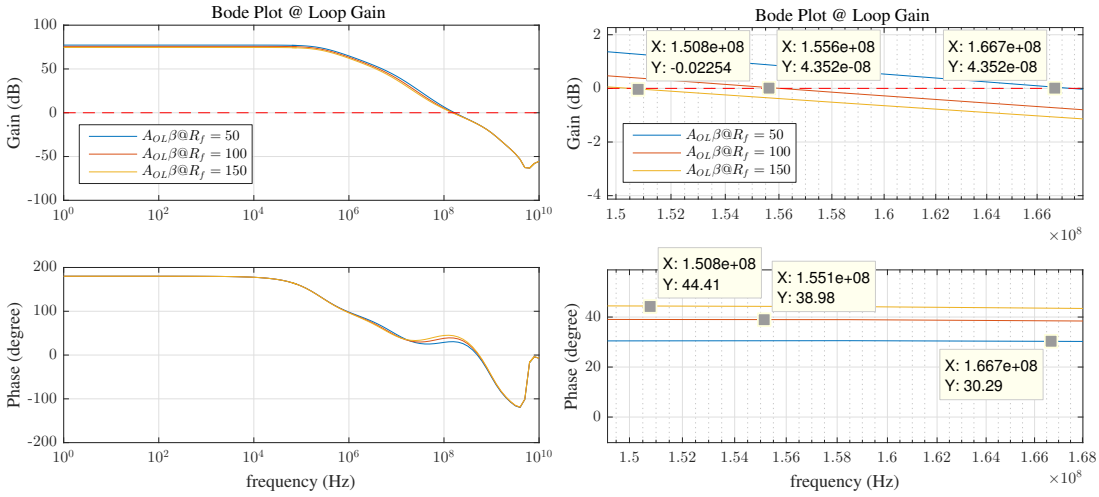
Moving towards to Figure 3.16, loop gain and phase are necessary to check the value of the phase margin. This analysis just confirms us the satability of the two previous ones (Figure 3.15) with more detailed information. Observing Figure 3.16b, the lowest value of the resistance corresponds with the lowest value of the phase margin. Thus, a phase margin of 30.29 degrees is obtained causing an overshoot and possibilities of instability in the circuit. For the other two cases, phase margin is not compromised any more.



(a) Magnitude Bode plot of open-loop gain and noise gain, parametric sweep of the feedback resistance

(b) Transient analysis, parametric sweep of the feedback ressitance

Figure 3.15: Indirect methods for stability analysis



(a) Bode plot - Magnitude and phase of the loop gain

(b) Zoom-in in 0 dB, phase margin measurement

Figure 3.16: Phase margin calculation for fixed-slope

Full-Flexible

As it is said before, for this configuration a digital potentiometer is used. It means that the parasitic capacitances of the device have to be taken into account for the stability analysis. From the data-sheet specifications:

$$C_A = 90pF, C_W = 40pF \quad @ \quad R_F = 10k\Omega \text{ (mid scale)}$$

This simple model can be used in SPICE simulations to predict circuit performance, such in our application, when the digital potentiometer is used as a part of the feedback network of an op amp. Considering parasitic capacitances, the new compensation network is recalculated. Then, only a feedback capacitance is added, taking a value of $C_F = 1.5pF$. Therefore, a parametric sweep of the feedback resistance is performed to ensure the stability of the circuit.

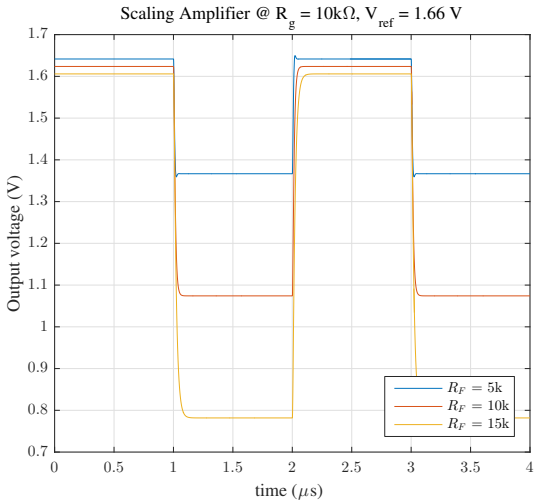


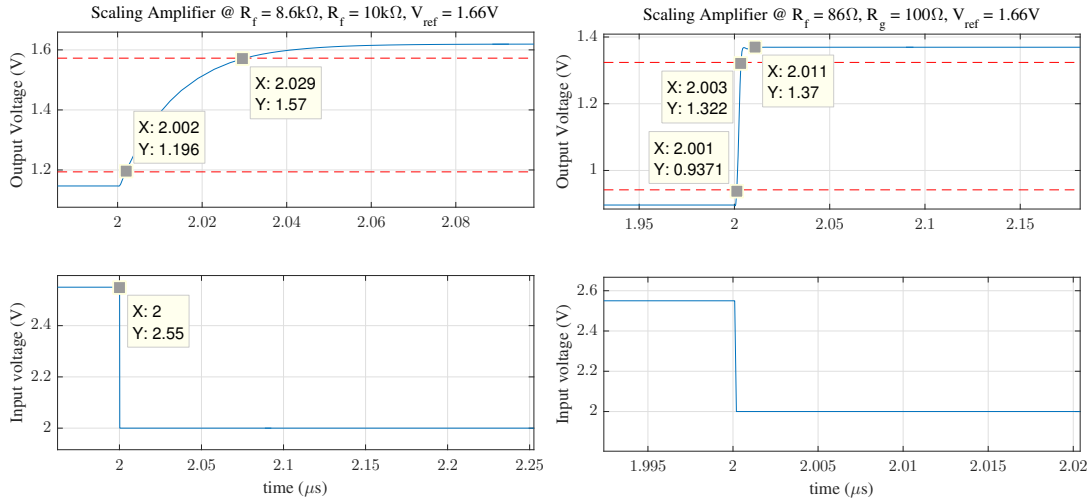
Figure 3.17: Transient analysis, parametric sweep of the feedback resitance

Figure 3.17 shows the output voltage within different slopes. In terms of stability, the three scenarios reveal a flat response, with an overshoot in the lowest value. In terms of speed, the rising time looks slower than the fixed-slope analysis. In the next section is explained in details.

3.4.3 Transient Analysis

The resistance in the path of a particular code, combined with the switch parasitic, pin, and board capacitances, creates an RC low-pass filter, which determines the maximum rising/falling time of the signal. For a small step signal, it can be calculated as:

$$t_{r/f} = 2.19 \cdot \tau \tag{3.2}$$



(a) Response time for full-flexible configuration

(b) Response time for fixed-slope configuration

Figure 3.18: Rising and settling time for both configuration: fixed-slope and full-flexible

Comparing the response time of the full-flexible with the fixed-slope configuration, it is slower because of the digital potentiometer (see Figure 3.18). The main values are summarised in table

3.2, where the penalty of using high resistance in combination with the feedback capacitance provokes a settling time of 40 ns. In short, full-flexible configuration win in reconfigurability but lose in speed.

Table 3.2: Comparison between Full-flexible, Fixed-slope times, calculated times

	Full-Flexible	Fixed-slope
Time constant - τ	$1.5pF \cdot 8.6k\Omega$ (13ns)	$19pF \cdot 86\Omega$ (1.6ns)
Rise/fall time	37 ns	2ns
Settling time	40 ns	11ns

3.5 Voltage-Controlled Current Source

After the explanation about the functionality of the circuit in the chapter 2, this section is intended to justify the component selection and to simulate its behaviour. A pair of operational amplifiers are chosen from Linear Technology, which they were the most suitable ones for our application.

LT1190 is an ultra-high speed operational amplifier, it is an ideal choice wideband signal conditioning, fast integrators, active filters, and applications requiring speed, accuracy and low cost. In addition, key features such as very fast slew rate of 450V/μs, unity gain- stable bandwidth of 50MHz and a 75 degrees of phase margin, makes it extremely easy to use [19]. LT1194 is a video difference amplifier optimized for applications requiring speed. It has uncommitted high input impedances and a fixed gain of 20dB. The LT1194's high slew rate 500V/μs, wide bandwidth 35MHz, make it ideal for driving our load [20].

Both operational amplifiers have a complex PSPICE model allowing us the simulation of the circuit in the most realistic conditions.

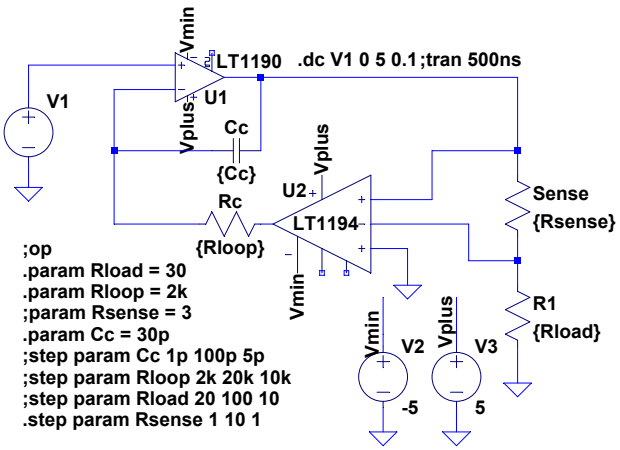


Figure 3.19: Schematic of the VCCS

Figure 3.19 represents the schematic of the voltage controlled-current source. The values of the passive components such as the sense resistor, load or compensation network are defined as variables since make easier the different type of simulations.

3.5.1 DC Analysis

Firstly, to full understand the behaviour of the VCCS, a parametric sweep of the sense resistor is performed. Thus, depending on the sense resistor the previous stage has to be designed in

concordance. Figure 3.20 shows a sweep from $R_{sense} = 1\Omega$ up to $R_{sense} = 10\Omega$. Bear in mind that sense resistor is the proportional factor that converts the input voltage into the output current.

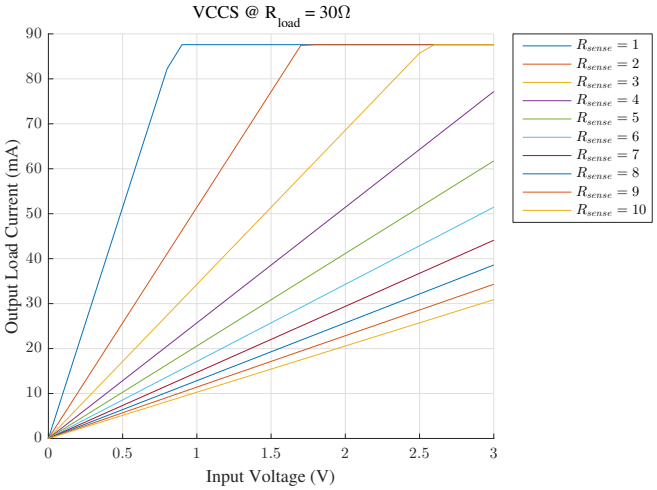


Figure 3.20: Parametric sweep of R_{sense} resistor and fixed load of 30Ω

The lower sense resistor, the lower input voltage is necessary to reach and saturate the output current with a maximum achievable value of 88 mA. Imaging two cases where a sense resistor is fixed either a value of 3Ω or 6Ω and the load takes different values. This is what is depicted in the Figure 3.21, this analysis is performed in order to test how dependent is the circuit with the load.

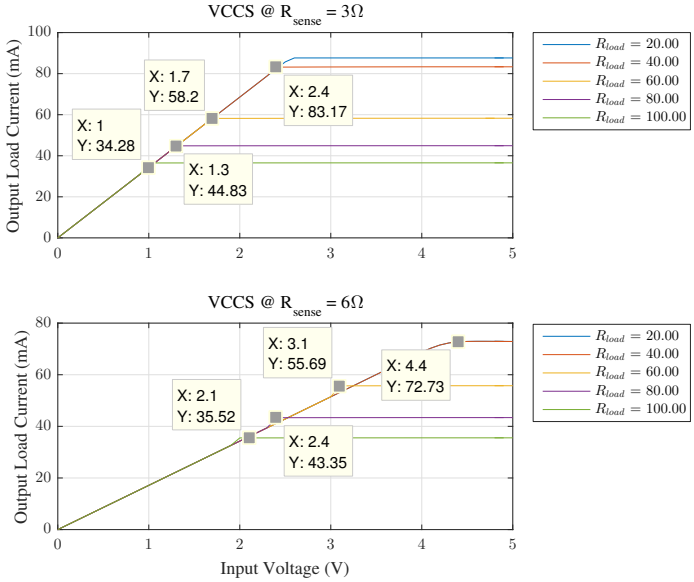


Figure 3.21: Parametric sweep of the load resistor, case for $R_{sense} = 3\Omega$ and $R_{sense} = 6\Omega$

The range of load resistances goes from $R_{load} = 20\Omega$ up to $R_{load} = 100\Omega$. As it is awaited, the slope is set by the sense resistor and the maximum current level before saturation is set by the load resistance. If we want a current source totally independent for that range of resistance, the maximum output current that it can provide is around 35 mA. Above that value one should care about the specifications of their load for a correct implementation of the circuit. For our purpose, we know that SOA load's not exceed a resistance of 30 Ω, it means that the maximum current

available would be around 83 mA for the first case or 60 mA for the second case.

3.5.2 Transient Analysis: Stability and Response time

Stability

Ringing is the unwanted oscillation seen in a voltage or current signal when the input or load is changed very quickly. If the controller cannot correct the output properly, overshoot and/or undershoot can occur, until it is damped out according to the damping factor of the system. The stability of the circuit is set by the combination of $C_c - R_{loop}$. The practical methodology to observe the effect of the compensation network to the output of the circuit is by means of a parametric sweep. Figure 3.22 depicts the step-response at the output depending on the feedback capacitance. From an initial value of 15pF up to a final of 50pF, the overshoot is reduced as long as the capacitance is increased. In the zoom-in graph, one can remark a significant ringing (5% overshoot) corresponding to the lower value (15pF). On the contrary, the maximum flat-response is achieved where the capacitance takes a value of 40pF.

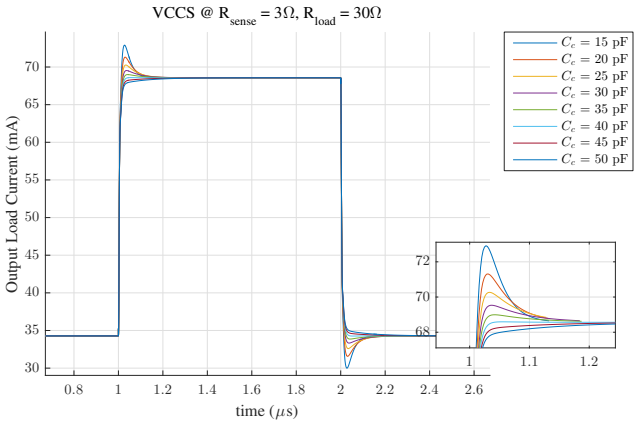
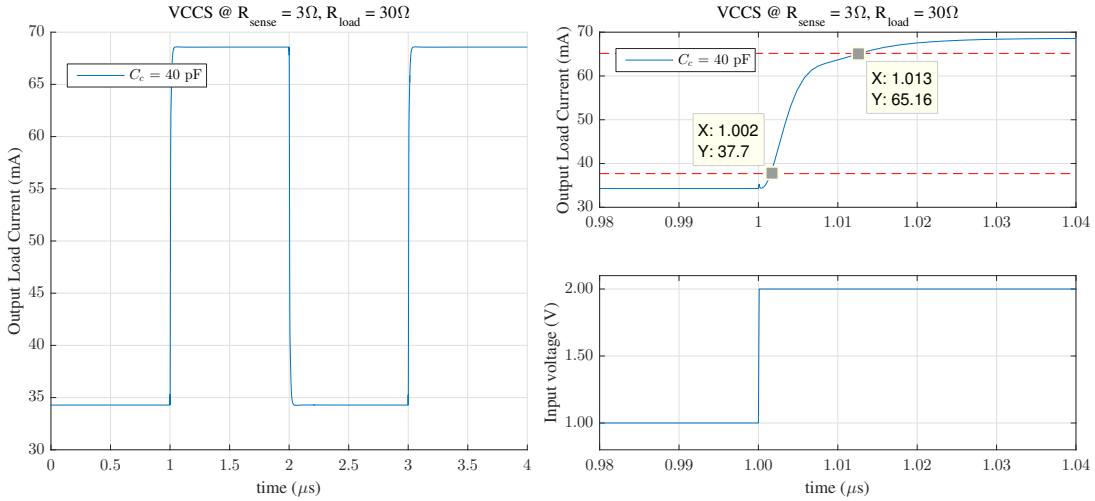


Figure 3.22: Parametric sweep of the compensation capacitance, case for $R_{sense} = 3\Omega$ and $R_{load} = 30\Omega$

Response time

Once the stability is solved, the response time of the circuit is calculated. The $2k\Omega$-40pF combination is the more stable, where the output signal is almost a perfect square waveform. Figure 3.23b shows a response time of the last stage, where a rising time of 11 ns and the a settling time of 30 ns are measured.



(a) Transient analysis, output load current

(b) Rising time and Response time measurements

Figure 3.23: Response time for an input voltage step of 1V up to 2V

Summarising all the responses time of each stage in Table 3.3. The longest rising time is given by the logarithmic stage. For the full-flexible configuration, the RC low pass filter caused by the high resistance increases the rising time respect the fixed-configuration. The last stage demonstrates a fast-response well below of the required time. Regarding the settling time, applying the criteria of 1% error band, again the log-amplifier is the lowest stage with a total of 50ns.

Table 3.3: Response time per stages, Scaling stage first time refers to fixed-slope and the second to full-flexible configuration

	TIA	LOG	SCALING	VCCS
t_r	20ns	40ns	3ns/27ns	11ns
t_s	30ns	50ns	11ns/40ns	30ns

3.6 Full design

Besides the individual simulation of each stage, a complete simulation of the circuit is investigated by using the schematic shown in the Figure 3.24.

The parameters are set to follow a transfer function of an SOA characterised in Chapter 5. In table 3.4 are shown the main values of the different passive components along the circuit (see Appendix A for a full description). Again, the simulation is only to have a general intuition of how the practical circuit will perform.

The next step is to show the biasing of the circuit as well as the response time of the signal, thus, a DC analysis and transient analysis are realized.

3.6.1 DC Analysis

Once all the parameters are well-known, it is straightforward to simulate the steady-state of the circuit. Choosing an input power from -40dBm up to -20 dBm, Figure 3.25 represents the output response of each stage. The transimpedance amplifier behaves as exponential function in front a logarithmic sweep. After this stage, logarithmic amplifier shapes with a linear response in dBm scale. The following stage, scaling amplifier, the slope and reference voltage take a value of slope

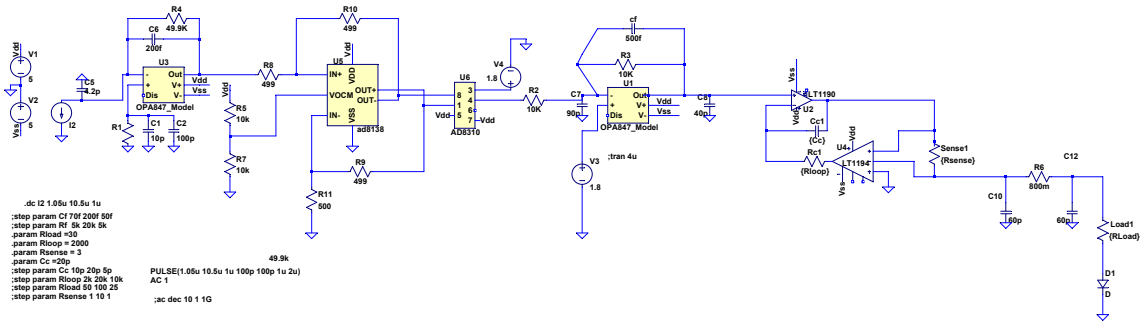


Figure 3.24: Schematic of the complete circuit

Table 3.4: Value of the parameters of the circuit

	TIA	LOG	SCALING	VCCS
R_F	$49.9k\Omega$	499Ω	$8.3k\Omega$	$2k\Omega$
R_G	-	499Ω	$10k\Omega$	-
C_F	200fF	-	1.5pF	40pF
R_L				30Ω
V_{ref}	-	-	1.65V	-

= 0.83 and reference voltage = 1.65. The output voltage keeps the linear shape for the whole range. Finally, the last stage of the circuit which is in charge to provide current to SOA, depicts the same trend as the previous stages.

In our case, the input power fed to the circuit depends on the coupler used in the line. Hence, a practical range where the circuit works properly is between -30 dBm and -20 dBm. In such a range, the maximum current that supply the circuit is 55 mA and the minimum current is 40 mA respectively. The most important aspect is that the current provided in the middle range keeps the linearity and allows equalization itself (section 2.1 for recalling).

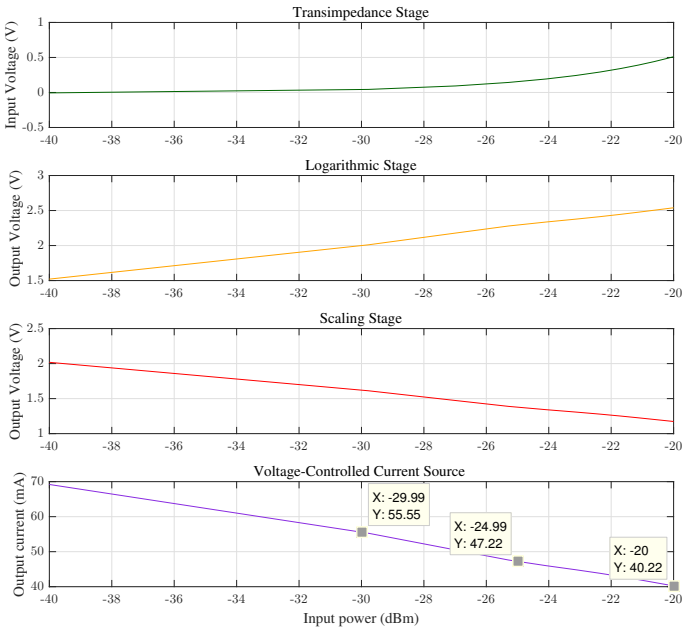


Figure 3.25: DC analysis, output response of each stage is illustrated.

3.6.2 Power Consumption

The power consumption is also a key factor for the next generation of data centers. For our design, a dual power supply is accounted, +5/-5 V. Figure 3.26 collects the power consumption for a range of input power between -40dBm to -30dBm. The positive power supply decreases as the input power increases, it is reasonable since the circuit has to provide higher current to equalize the lowest optical power to the highest one. The consumption for the positive power supply is higher than the negative since the logarithmic stage only need a single power polarisation. Besides, in this estimation, the digital potentiometers are not count due to the lack of a spice model. In short, the average power of 1.37W is calculated for all operations of the circuit.

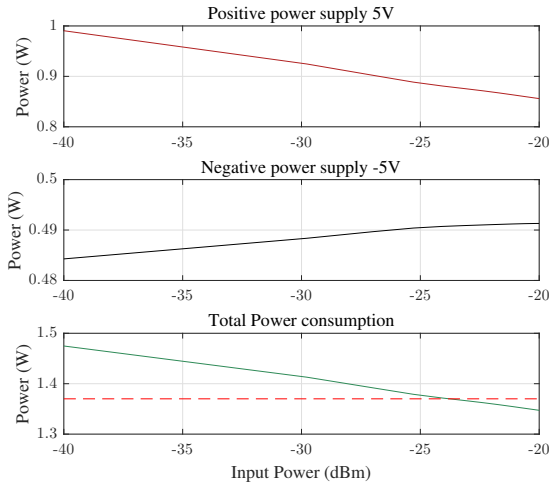
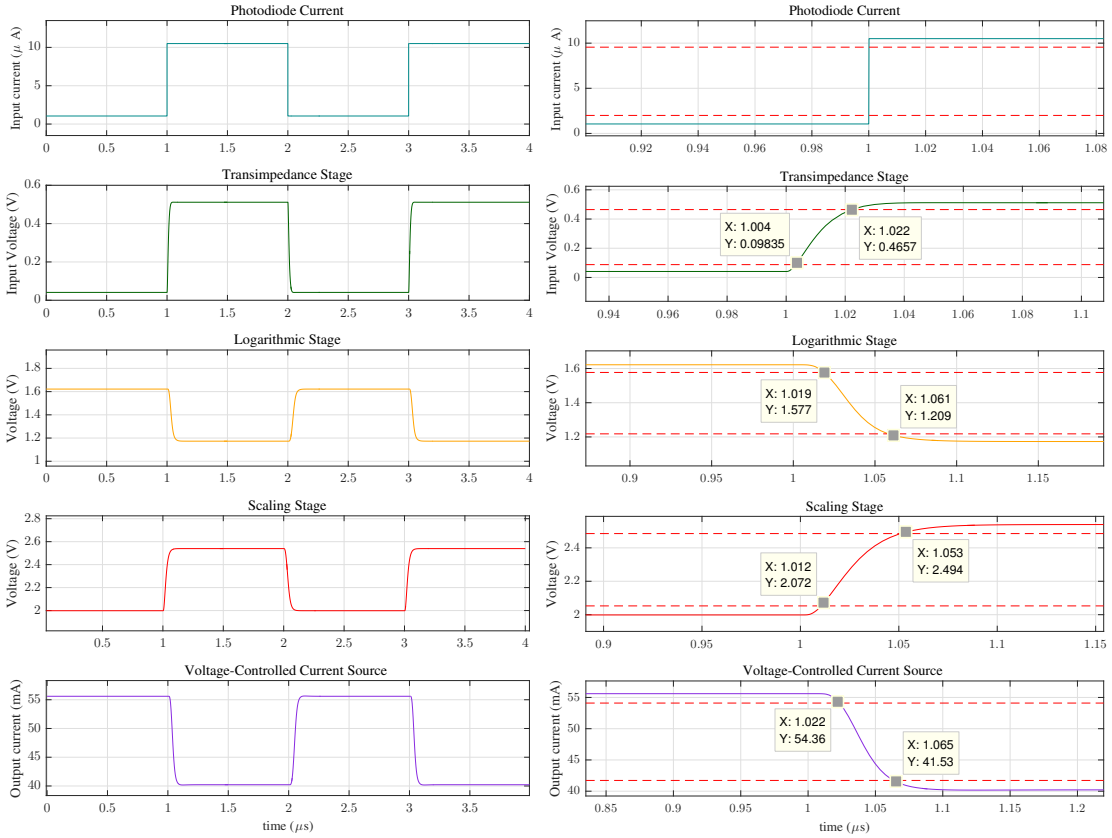


Figure 3.26: Power consumption of the circuit

3.6.3 Transient Analysis

This last analysis is crucial since the objective of all the design was the response time, pushing it beyond the limits to achieve the fastest plausible circuit. Instead of using the simplest solution, whose would be a true-log stage with the photodiode directly connected (but response time would have compromised), RF-Log stage is used in the middle of the two stages in order to have the correct design in the minimum response time. Then, a transient simulation is analysed in each stage. The scenario is a transition between two packets at the maximum difference, -30 dBm and -20 dBm. In Figure 3.27 is plotted the output response of the four stages and the reference input current simulating the pulse of the photodiode.



(a) Transient analysis, input current equivalent to a range of -30dBm up to -20 dBm power

(b) Zoom-in of the signals, response time measurement

Figure 3.27: Transient analysis of the whole design

Figure 3.27a shows the overall behaviour of the circuit, thanks to the stability analysis and the correct values of the compensation network, the signals shapes with a smooth and flat response along all the circuit. Zooming in the signals, the rising time and setting time are measured. The bottleneck of the circuit is the logarithmic stage. After that stage, the response time remains constant in all the circuit (see Table 3.5).

Table 3.5: Response time per stages

	TIA	LOG	SCALING	VCCS
t_r	18ns	40ns	41ns	43ns
t_s	40ns	100ns	100ns	100ns

3.7 Summary

In this chapter, the simulation and components selected of the circuit have been presented. Benefiting from the analog design, high-response and low power consumption can be achieved by employing four stages in the whole design. Simulation models have been built in LTSPICE environment and realistic models of the components have been used. In the third stage, scaling amplifier has been demonstrated in two different prototypes. For full-flexible prototype, digital potentiometers are shown in the feedback loop as well as the reference voltage. In Chapter 5, the control software is explained and implemented. Performance comparisons between two prototypes indicate that the penalty comes from the low-pass filter of the digital potentiometer. Assessment results show 100 ns response time for the whole circuit, where the logarithmic stage is the bottleneck imposing the slowest settling time. Steady-state behaviour has been demonstrated for a specific scenario in Section 3.6. In addition, power consumed by the prototype is around 1W and a linear increase with the in-line SOA channels is expected.

Chapter 4

Design of the PCB Layout

In this chapter, the design and layout of the employed fast analog equalizer is introduced. Moreover, an extra circuit is deployed since it is only a stage of the equalizer (VCCS) and another current driver designed by my co-advisor M.Wang. In total, three PCB are presented: Fixed-slope configuration, full-flexible circuit and tunable laser driver. In the following, section 4.1 presents an introduction about PCB design. The footprint design of the components is explained in the section 4.2, followed by the section 4.3 which provides the detailed schematic design for each circuit. In section 4.4, the layout of the PCB is reported. Explaining the number of layers, power planes and the routing.

4.1 Introduction

Once the components are selected and the simulation is performed, the next step is to proceed with the PCB layout design. Figure 4.1 shows the PCB flow chart design which was followed for our work. Information about all the components is found in each respective data-sheet, creating the component symbol following the number of pins is our first real task after the simulation. Afterwards, schematic design ensuring properly every node is fundamental. Before transferring all

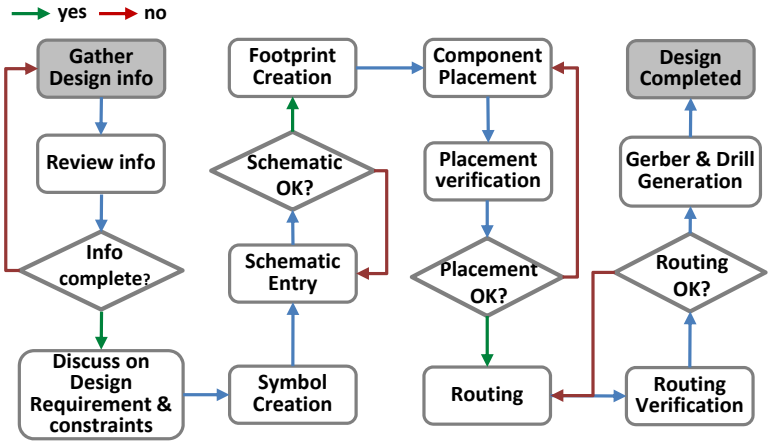
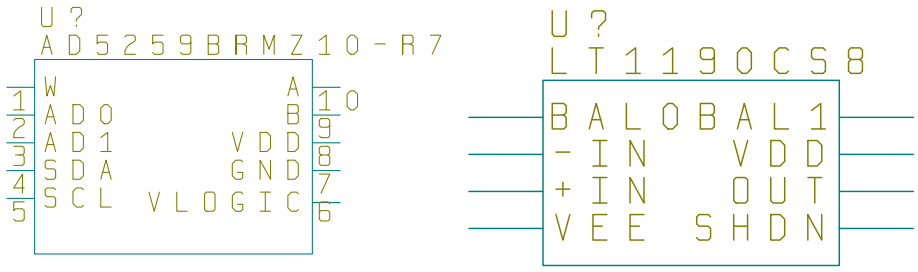


Figure 4.1: PCB flow chart design

the schematic to the PCB layout, the footprint of the components is designed. For the placement and routing, the software helps you with invisible lines in the connections. Anyway, achieving the optimal routing is a challenging task since sometimes it is simply impossible and the less critical

path is sacrificed. Finally, the generation of the outfiles, gerber and drill files, is sent to the PCB production company.



(a) Symbol for AD5259, digital potentiometer (b) Symbol for LT1190

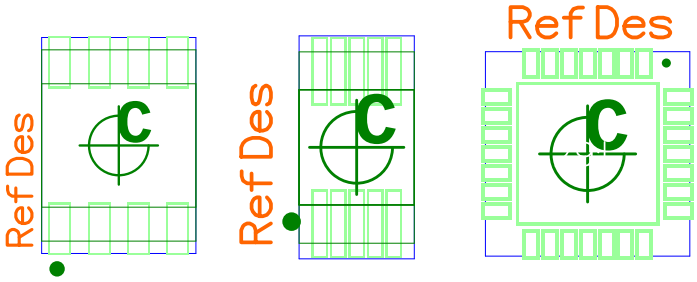
Figure 4.2: Symbol creation

Figure 4.2 shows two examples of the schematic symbols. Figure 4.2a depicts the digital potentiometer which controls the reference voltage. Figure 4.2b refers to an amplifier of the voltage-controlled current source. The symbols are created as convenient for my design.

4.2 Footprint design

Using the manufacturers data-sheet, you may be lucky enough to be presented with footprint pattern dimensions. Typically, the data-sheet will just reference a footprint name which you must then source the dimensions for.

A padstack is the geometrical description of each pin of a PCB. It is the exposed PCB surface where components are mounted and soldered. There are 2 types of padstacks; through-hole or surface mount padstacks. After the creation of the padstacks, one can start with the design of the footprint. Normally, the software has a footprint wizard tool which helps to the designer with some patter-generation. However, it is only for standard packaging such as SOIC-8. Figure 4.3 illustrates three different packages for the design, where Figure 4.3a is the footprint of the operational amplifier OPA847, Figure 4.3b of the digital potentiometer and Figure 4.3c of the current driver.

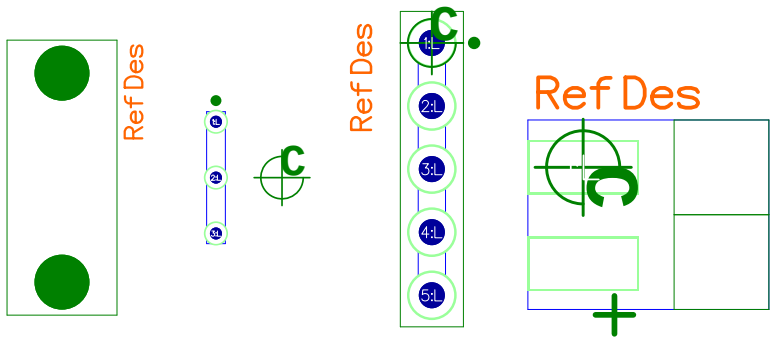


(a) SOIC-8 (b) MSOIC-10 (c) QFN

Figure 4.3: Package types

Moreover, some full-custom footprints are designed exclusively for this PCB. For instance, Figure 4.4a represents the footprint for the photodiode. It is attached horizontally on the edge of the PCB, the dimension of the case and the three pins are included in this footprint. Regarding Figure 4.4b, it shows the 5-connection header for the power supply and communication system. A

SMD double pin header is chosen for the connection between the device and the SOA (see Figure 4.4c)



(a) Photodiode (b) 2.54 mm 5-Header (c) SMD Header - SOA connector

Figure 4.4: Custom footprints

4.3 Schematic design

The final output of schematic design is a more informational piece than an outright physical design of a circuit. It shows what is connected to where and gives a good overview of the inner workings of the circuit.

4.3.1 Fixed-slope configuration

This schematic is exactly the same than the one of the section 3.24 including the symbols for the connectors and the photodiode. (see Appendix B)

4.3.2 Full-flexible configuration

The replacement of the analog potentiometer, the two digital ICs and the respective connections for the communication are the only difference respect to the previous schematic. (see Appendix B)

4.3.3 Tunable laser driver

This circuit is just a copy of the last stage analysed in the section 3.5. Additionally, two more voltage-controlled current source with fast on/off mode but lower transient time is added. (see Appendix B). This design is intended for driving a tunable laser.

4.4 PCB Layout

4.4.1 PCB Stack-up

A 4-layer PCB is the best option for this design. One of the major differences with boards that have more than two layers is the ability to alter what layers are actually connected by vias.

1. Signal plane
2. Ground plane

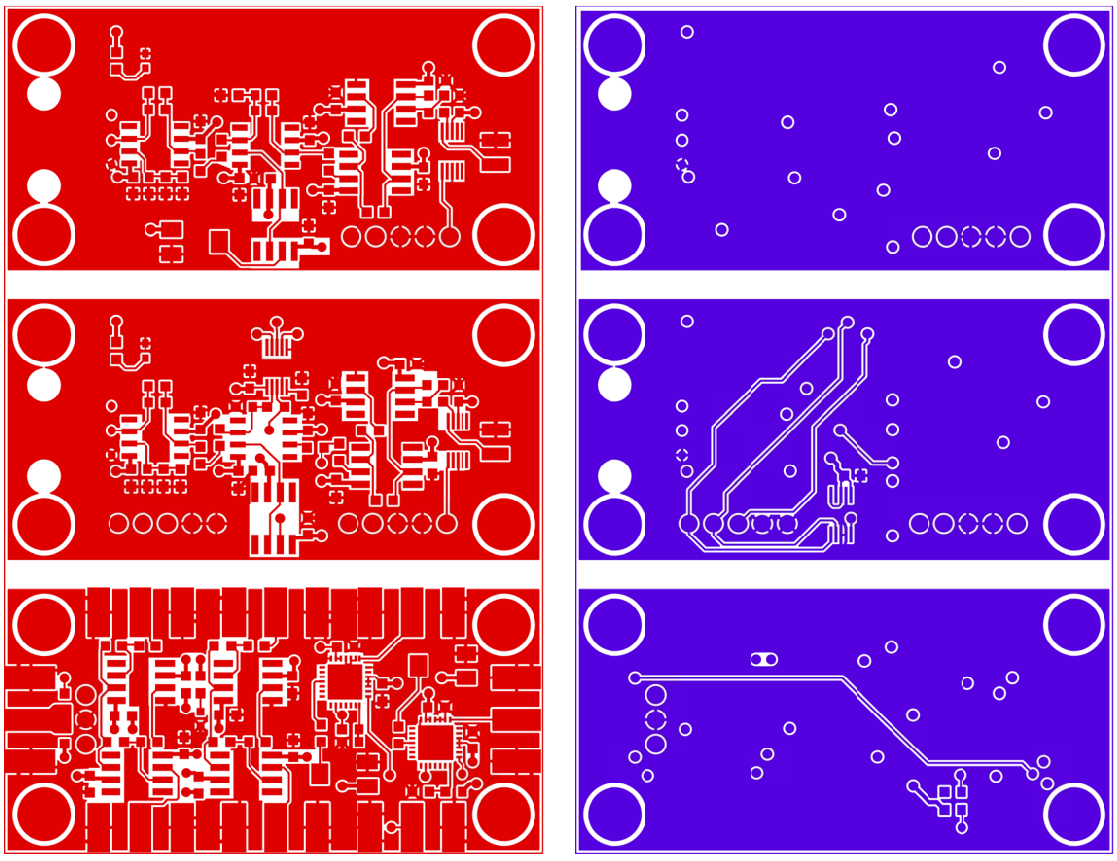
3. Power Plane
4. Signal Plane

4.4.2 Signal plane

Benefiting from the double-sided layout, loading components on both sides of the PCB make possible a compact design and same size board for the three different prototypes. Figure 4.5 represents the signal layer layout. The first design is refers to the fixed-slope configuration. The main differences between the full-flexible design are:

- The ratio of resistance is replaced by a digital rheostat.
- The analog potentiometer is replaced by a digital one.
- An extra 5-pin header is added in order to communicate with the two digital potentiometers.

As a consequence, the placement of the one of them is on the bottom layer (see Figure 4.5b). All the connections for I2C protocol are also routed in the that layer, allowing a compact design. For both prototypes, each stage has a test point which can be disconnected from the others to test it individually.



(a) Top view signal layer

(b) Bottom view signal layer

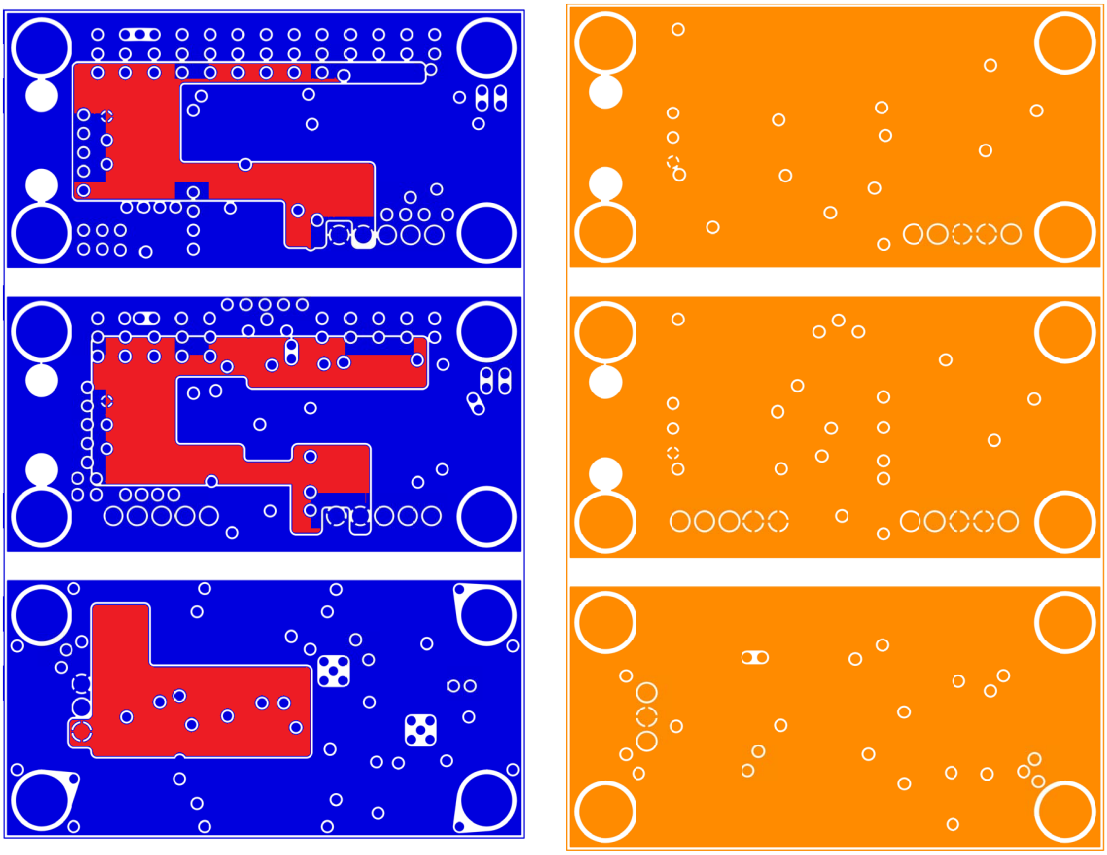
Figure 4.5: Signal layer

The last design corresponds to the tunable laser driver, where four voltage controlled current driver are placed side-by-side. The I/O signals are connected via SMA, which is the connector

used by FPGAs. Two of circuits have an enable pin allowing on/off gating. For the matter of testing, a SMD zero resistance (jumper) is placed to V_{DD}, assigning a high value to the pin. Also, a control signal is routed across all the bottom layer.

4.4.3 Power plane

Using power planes reduce dramatically the power wiring inductance and impedance to the components. On a multilayer board with positive and negative power supply, it is common to dedicate one layer to the ground and the another one to the double power supply. For our design, $\pm 5V$ is the power supply of the circuit and some components are only single-supply, +5V-GND. Figure 4.6a shows the power layer split in two different planes. The red plane is related with the negative power supply while the blue plane to the positive. Thus, shaping the power plane as convenient, the power tracks are only a vias with its decoupling capacitor. Figure 4.6b illustrates the ground plane of the design, one layer is completely dedicated to it. A complete ground layer provides a low impedance connection of all ground points for low noise and small potential differences between components connected to ground.



(a) Power layer

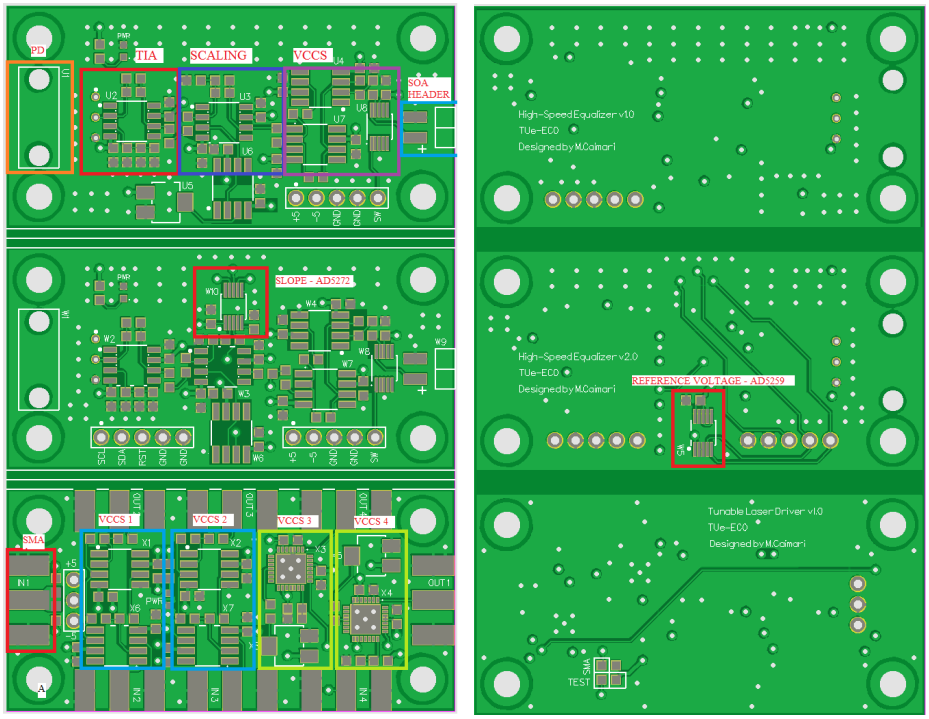
(b) Ground layer

Figure 4.6: Power layer

4.4.4 Final layout

After verifying all components and completing the final PCB checks, the Gerber files are generated and uploaded to the board manufacturer's web page. The last verification can be done on-line before placing the order. This data verification tool also provides a general overview of the design.

Figure 4.7 shows the final layout of the PCB, silkscreen and solder-mask included. Moreover, on top and bottom layers is included a ground plane and connected each other (multiple vias around the PCB) to reduce the noise and crosstalk. Table 4.1 shows the dimensions of the design as



(a) Final layout, top view

(b) Final layout, bottom view

Figure 4.7: PCB view generated by the manufacturer

well as the patter class. In total, 5.5cm x 8,7cm is the size of the three boards. Leaving a space between them in order to cut it after the manufacturing process.

Table 4.1: Specifications of the PCB

Board technology	
Pattern class	4
Outer layer trackwidth	0.200 mm
Outer layer isolation distance	0.200 mm
Outer layer annular ring	0.150 mm
Inner layer trackwidth	0.250 mm
Inner layer isolation distance	0.200 mm
Inner layer annular ring	0.150 mm
Board definition	
PCB width (X)	55.6mm
PCB height (Y)	87.6mm
Number of layers	4

4.4.5 Additional Stage: bread-board design

As it is explained in Chapter 1, a mathematical concept of equalization was taken as a correct and it was not. The principal consequence is the design of the PCB, where it does not contemplate the logarithmic stage. For external reasons, a new PCB design was not a possibility, so a new solution came out. A breadboard, including the log stage was fabricated. Figure 4.8 shows a sketch used as a guidance when the soldering and placement of the components.

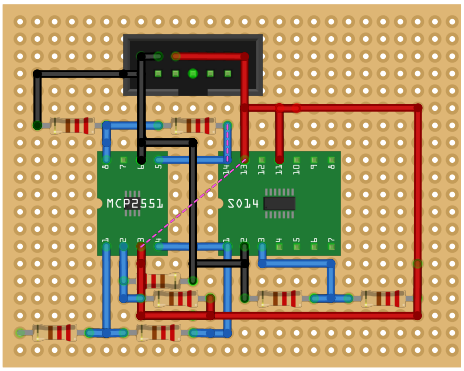
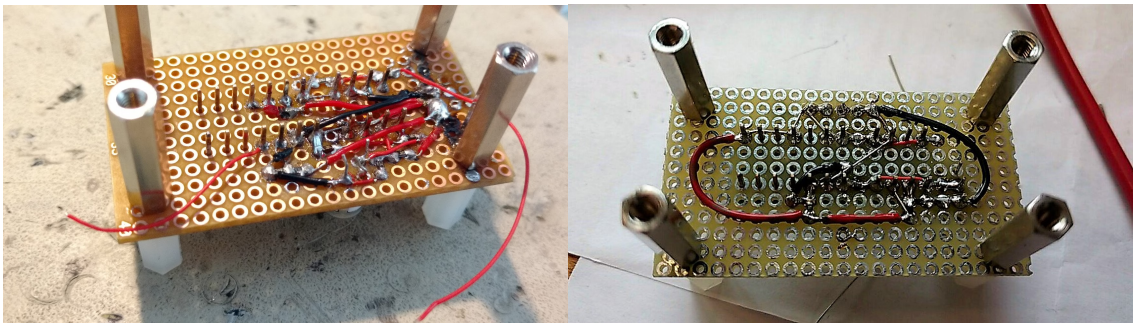


Figure 4.8: Breadboard, sketch of the log stage

To do so, a breadboard is cut in the same dimensions than the full-custom PCB and it attached afterwards. In addition, SMD-to-throughhole adaptors are necessary to work with the single-to-differential op-amp and the log-amp. Besides, the through-hole resistance of the sketch are substituted for its SMD counterparts. Figure 4.9 introduces the two iterations of placing and soldering. Recalling section 3.2, an unbalanced circuit has consequences on the linearity of the circuit. Then, a careful prototype has to be developed. For instance, a first soldering prototype was asymmetrical causing offset issues on the stage and inaccurate results in steady-state (see Figure 4.9a). A second iteration was needed, where the symmetry and clearness are cautiously conserved (see Figure 4.9b)



(a) First soldering (b) Second soldering

Figure 4.9: Bottom view from the breadboard log stage

4.5 Summary

In this chapter, three designs have been demonstrated: Fixed-slope (High-Speed Equalizer v1.0), Full-flexible (High-Speed Equalizer v2.0) and VCCS drivers (Tunable Laser Driver 1.0v) (see Appendix C). Symbol, cells and parts of all the components in the schematic have been correctly designed. Then, the schematic for each circuit has been created following the previous simulation design, adding the connections for the power supply and I/O connections. Concerning PCB stack-up, four-layer ordering such that it adequately delivers the required signal performance and power integrity at the clearest and most compact design. The top and bottom layers are exclusively for signals, the second layer is the ground plane and the third layer is the power plane. In the power plane, positive and negative power supply are used, splitting the plane into individual planes, as is described in section 4.4.3. Furthermore, an extra stage has been built in a bread-board design. After two iterations, the circuit works properly taking into account the limitations of the board. Finally, a picture of the full circuit is shown in Figure 4.10, where the value of the components are shown in Appendix C.

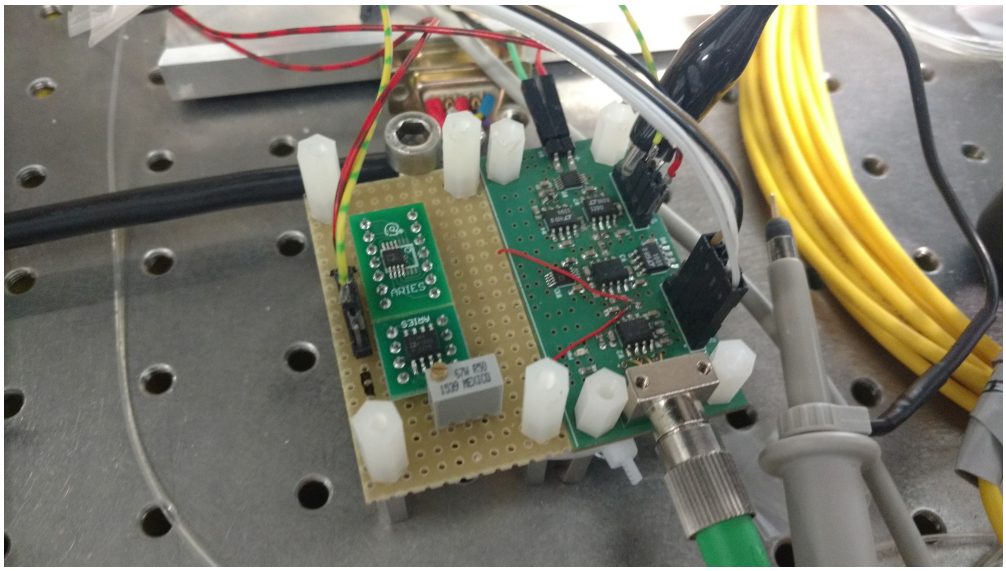


Figure 4.10: Final prototype

Chapter 5

Testing and verification

In this chapter, testing and verification of the prototypes are presented. As described in Chapter 3, each stage is analysed individually by means of DC/Transient analysis, comparing the results with the simulation. In the following, the steady-state response is described in the section 5.1. The transient analysis is detailed in section 5.2, where a function generator is used to observe the electrical signal response. Experiment with modulated data (PRBS sequence) is introduced in section 5.3, testing the behaviour of the circuit with practical data. Additionally, the full-flexible configuration is detailed in section 5.4, followed by the control-plane and experimental results.

5.1 DC Analysis: Operation point

The next challenging point is to check that the practical responsivity of the photodiode matches with the data-sheet value. Figure 5.1 shows the setup for this analysis.

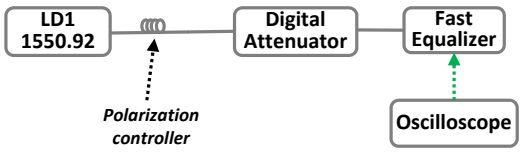


Figure 5.1: DC experimental set-up

In the first experiments the results of the practical values and the mathematical ones did not match. The slope was different, so it has something to do with the photodiode. Mathematically, the output of the first stage follows :

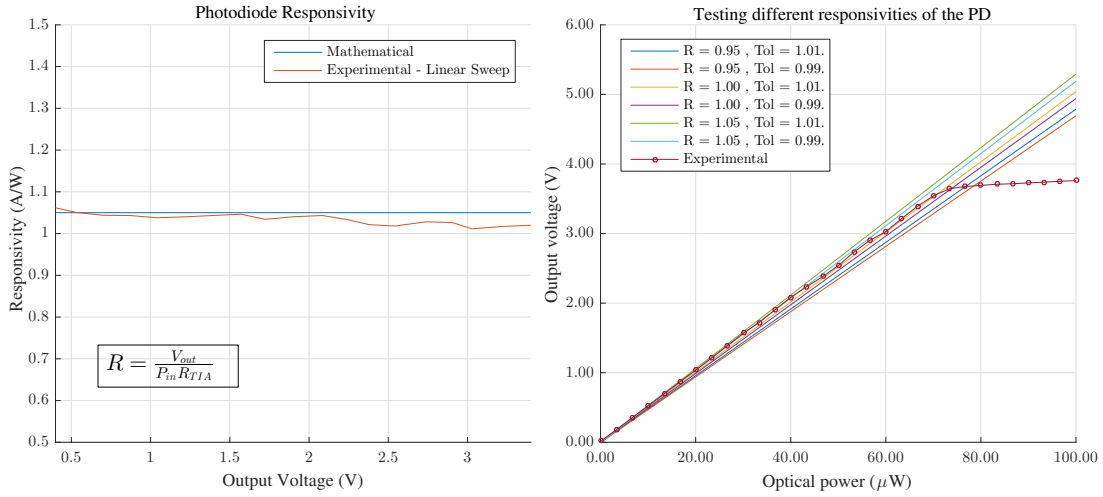
$$V_{TIA} = R_F I_{PD} = R_F R_{PD} P_{in} \tag{5.1}$$

where R_F is the feedback resistor, R_{PD} is the responsivity of the photodiode and P_{in} is the input power. So, the feedback resistance and the input power are well-known parameters, then by using the data of the output voltage of the experimental measurements we can obtain an approximate value of the responsivity of the photodiode:

$$R_{PD} = \frac{V_{TIA}}{P_{in} R_F} \tag{5.2}$$

Figure 5.2a shows the responsivity calculated with the equation 5.2. One can observed that it is slightly higher that the data-sheet value (R = 0.95 A/W) [21]. The mathematical line is constant since it is the ideal case (R = 1.05 A/W). The experimental line of the responsivity

changes along the different output voltages but also maintaining a trend close to the ideal. Figure 5.2b depicts the ideal value of the output voltage of the transimpedance amplifier depending on the responsivity of the photodiode and the tolerance of the feedback resistor. Finally, the result fits with the calculated responsivity. Once the responsivity is fixed, the mathematical value and simulation are repeated in order the fit the curves to the experimental one.



(a) Photodiode responsivity

(b) Parametric sweep with different responsivities

Figure 5.2: Practical responsivity of the photodiode

5.1.1 Stage 1: TIA

The first stage is in charge of the optical-to-voltage conversion. Figure 5.3 represents the output voltage of the stage, it increases linearly in a logarithmic scale, where the minimum value 6mV corresponds to an input power of -40 dBm and it saturates at -12 dBm with an output voltage of 3.28V. The experimental measurement follows the simulation graph as close as possible confirming that the spice models of the simulation are well-designed.

As a first conclusion, the range of input power that the circuit can work with is 28 dB, more than enough for a dynamic range of 10 dB. In that range, the output voltage goes from 6mV up to 3.28V, so having total voltage range of 3.22V at the output of the circuit.

5.1.2 Stage 2: Log Amplifier

The second stage converts output voltage of the transimpedance amplifier into a linear-in-dB response. Regarding the experimental setup, it was arduous and troublesome since the addition of that stage was a posteriori. In the Chapter 4 is shown some pictures of the implementation of the stage. Figure 5.4 represents the steady state response of the log stage, it is compared with the simulation and the mathematical curves as the other stages. One can observe that the experimental curve follows the simulation curve up to certain point. Although the DC simulation starts from a low voltage $100\mu V$ to 1V and the experimental curve starts from 5 mV due to the limitations of the voltage calibration instrument, then it enough to prove the behaviour of the stage. Moreover, the practical log-amplifer reaches higher output voltage before the saturation (2.9 V). The linearity is preserved in all the input voltage range with some errors at the lower voltages.

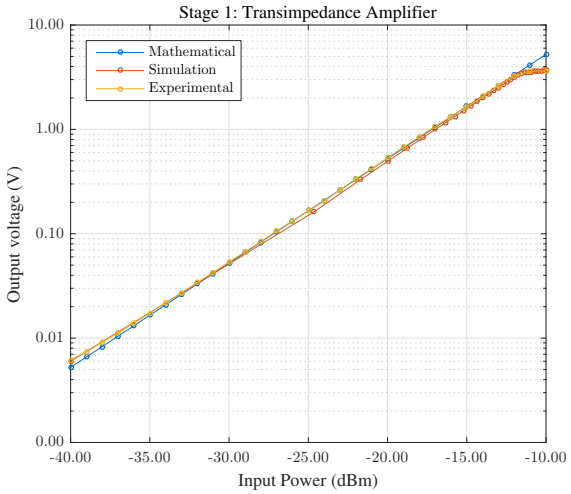


Figure 5.3: Output voltage of the transimpedance amplifier, comparison with simulation and mathematical model

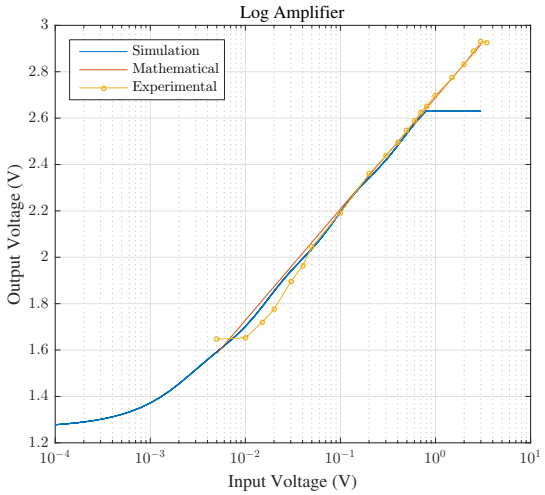


Figure 5.4: Log stage, DC Analysis

5.1.3 Stage 3: Scaling Amplifier

The second stage is in charge of scaling the output voltage of the transimpedance amplifier to the input voltage of the voltage-controlled current-source. All graphs show a linear behaviour as well as the first stage. The slope is negative since we need to invert the signal to provide the maximum current at the minimum voltage. Nevertheless, the simulation and experimental curves saturate around zero voltage because of the input voltage. The output voltage range goes from 2.2V up to 0V, that is for a fixed ratio of resistances and offset voltage. Bear in mind that a second design is proposed to change the slope and the offset via PC.

5.1.4 Stage 4: VCCS

The last stage is the voltage-controlled current source, where the input voltage is converted to an output current. The current measured in that stage is when it is loaded with a resistance. For a DC analysis it is a good approximation instead of using the SOA load, but not for a transient analysis, which is explained in the transient analysis section.

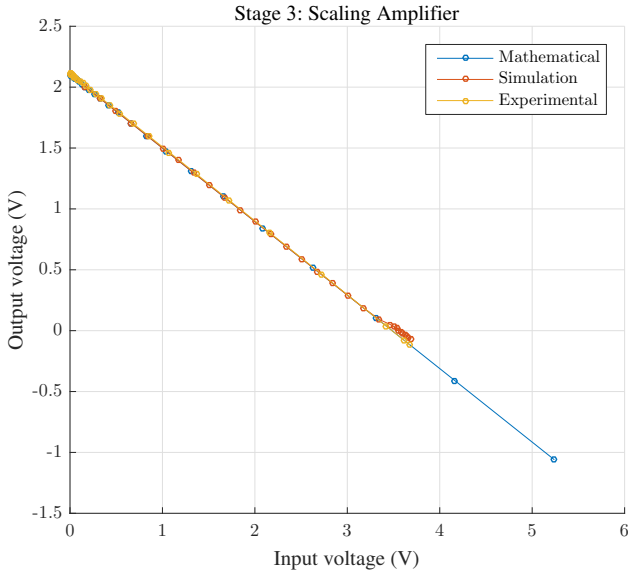


Figure 5.5: Output voltage of the scaling amplifier depending on the output voltage of the first stage, comparison with simulation and mathematical model

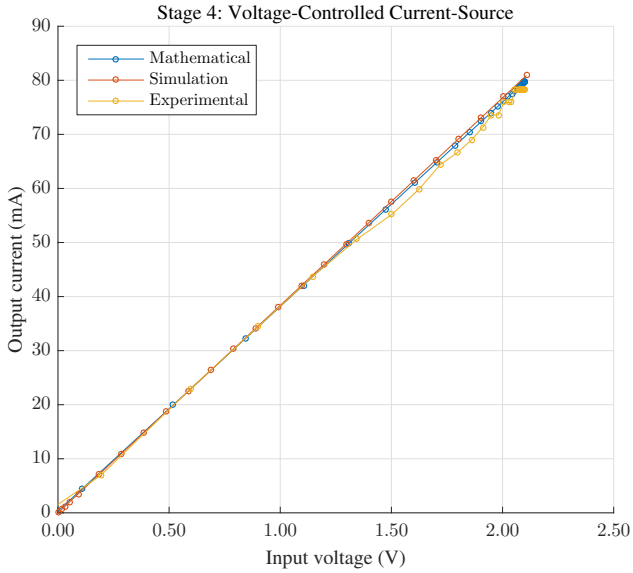


Figure 5.6: VCCS stage, output current against the output voltage of the scaling stage.

Figure 5.6 represents the output current of the circuit. In the chapter 2 is explained how the maximum current can be set at higher values and up to which load the current source is independent. As the previous stages, the behaviour of the stage is linear but the experimental curve has some difference of current due to an instrumental error.

5.2 Transient Analysis: Response time

In this section response time of each stage is analysed individually. Either the output voltage from a function generation or the optical power of the bit pattern generator are square waveform without data, ideal clean signals to prove that the behaviour of the stage is the expected one.

For the first stage, a optical input source is used, however, the other stages are analysed with a function generator and an electrical square wave signal.

5.2.1 Stage 1: TIA

In this first stage, an optical square signal is fed to the photodiode. There is no data in this experiment, so the input signal is clean enough to focus only in the response time of the stage. Figure 5.7 shows a smooth and flat response for an input power between -30dBm up to -20dBm. Zoom in the signal, the rising time is 33 ns and the settling time is 72 ns. Comparing with the simulation (20 ns / 72 ns), it is acceptably close to the those values since a small-signal step does not put the operational amplifier in a slew-rate limit.

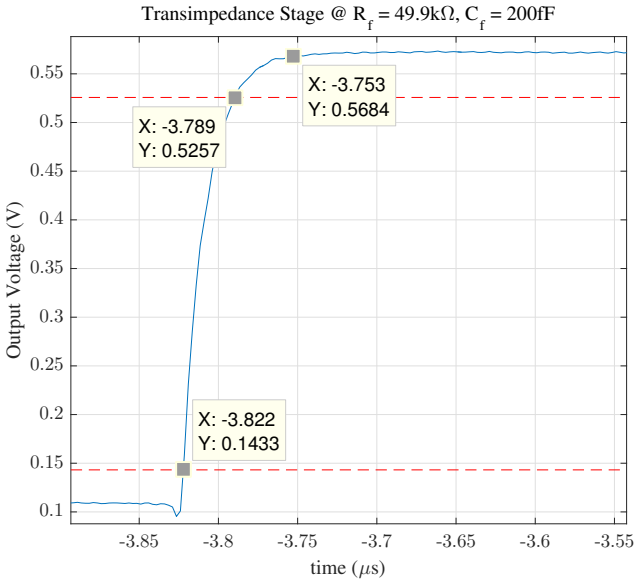


Figure 5.7: Response time of the first stage

5.2.2 Stage 2: Log Amplifier

In this stage, the response time of the logarithmic stage is studied. In Figure 5.8 is shown the output voltage respect to the input voltage. For a large-signal step, the rising time is counted as 20 ns, it is tolerably close to the specifications given in the data-sheet (15 ns). Regarding the settling time, with a error band of 1%, a value of 60 ns is measured. A recommendation from the manufacturer is to add a feedback capacitance to smooth the ringing, in these measurements is added with a value of 1pF, achieving the flattest available response.

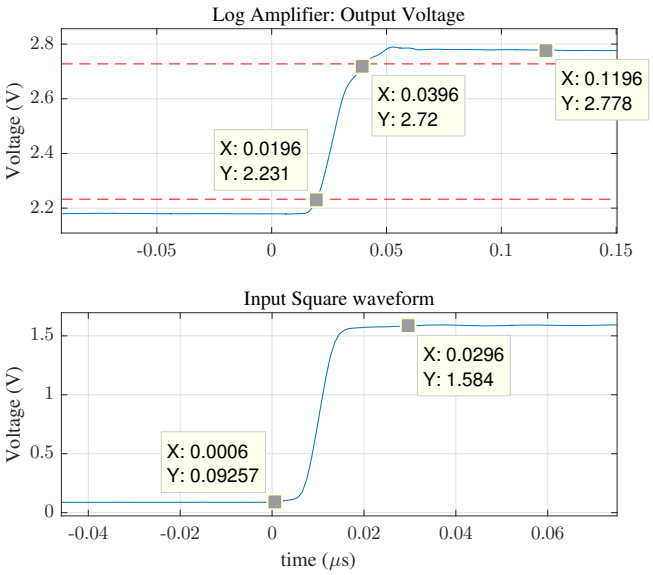
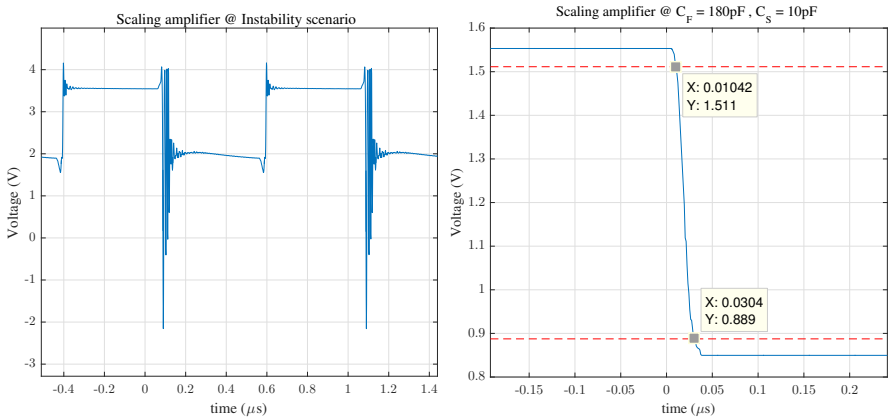


Figure 5.8: Transient analysis of the log amplifier

5.2.3 Stage 3: Scaling Amplifier

This was the most problematic stage together with the VCCS stage so far. Stability issues has been discovered during the debugging of the circuit. Firstly, working with the fixed-slope circuit had some drawbacks. Along the testing part, the slope has been changed many times, i.e , the value of the resistances. Consequently, the values of the compensation network have been replaced to achieve the smoothest and flattest signal. Figure 5.9 shows the case of the fixed-slope circuit, where it is fixed by the ratio of two SMD resistance. The first plot shows an example where the circuit suffers of instability, the ratio of resistance was changed but not the capacitance (Figure 5.9a). In the next plot, the stage is stable and optimized for the flattest response. This corresponds to a set of capacitances of $C_F = 180pF$ and $C_S = 10pF$. Thus, the rising time for the fixed-slope configuration takes 2ns and 5 ns for the settling time.



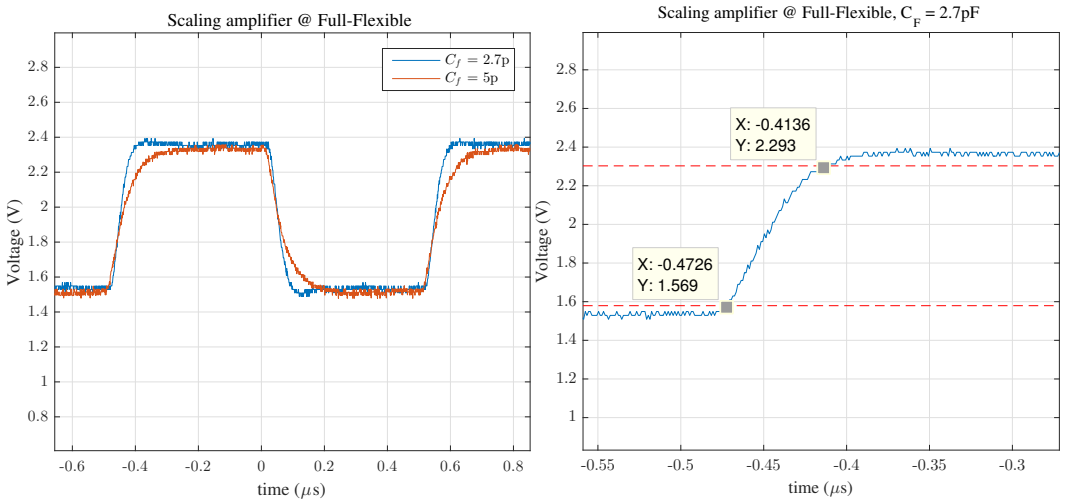
(a) Instability scenario, circuit starts to oscillate with a transient signal

(b) Response time of the fixed-slope scaling stage

Figure 5.9: Scaling Stage for the first prototype

In this case, scaling stage with digital potentiometer is presented (see Figure 5.10). As it is

studied in Chapter 3, digital potentiometer introduces a higher constant time due to the high resistance. Figure 5.10a illustrates the effect of the feedback capacitance on the signal. A 5pF value undershoot the signal making it slower, after different values, a 2.7pF capacitance is selected to reach the best shape of the signal.



(a) Transient response - list of two capacitance were tested

(b) Response time for full-flexible configuration

Figure 5.10: Scaling stage for full-flexible circuit

Following the previous explanation, the rising time for the full-flexible configuration takes 60 ns (see Figure 5.10b). Comparing it with the simulation (28 ns), it rises slower because the feedback resistance necessary to compensate the signal is slightly higher (2.7pF) in front of 1.5pF. Moreover, the rising time could be slower depending on the selected value of the wiper.

5.2.4 Stage 4: VCCS

The last stage of the circuit, where the voltage is converted to current, is analysed in terms of dynamics. This stage is highly sensitive and difficult to analyse. The evolution of the signal changes depending on the load that is used. SOA is not more than a PN junction, its resistance varies with applied current. To stabilise the signal at the output of the VCCS, a resistance is added in series to SOA in order to keep constant the load for the circuit. The results of this explanation are shown in Figure 5.11. The rising time of the last stage takes 16 ns, meanwhile, the settling time takes 100 ns after the ringing of the signal.

All in all, the timing of each stage is collected in the table 5.1. On the contrary of the simulation, the bottleneck is the practical circuit is given by the scaling stage for the full-flexible prototype. Since the simulation was made with the theoretical value of the parasitic capacitances, it was only an approximation. Hence, the lowest rising time corresponds to 60 ns and to the full-flexible configuration. It is true that the settling time of the different stages also takes 100 ns, but it is not revelatory until to connect the whole device together.

Table 5.1: Rising and settling time per stages

	TIA	LOG	SCALING	VCCS
t_r	33ns	15ns	2ns/60ns	16ns
t_s	72ns	60ns	5/80ns	100ns

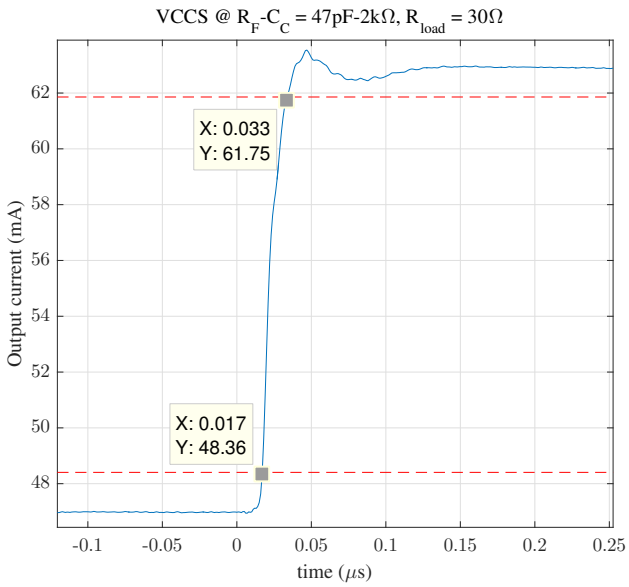


Figure 5.11: Transient analysis of the VCCS

5.3 Experiment with packed-based PRBS

The purpose is to test a PRBS pattern at different data rates (10Gbps/20Gbps/40Gpbs) with the following setup (see Figure 5.12). The prototype used in this experiment is the High-Speed Equalizer v1.0, without log-stage.

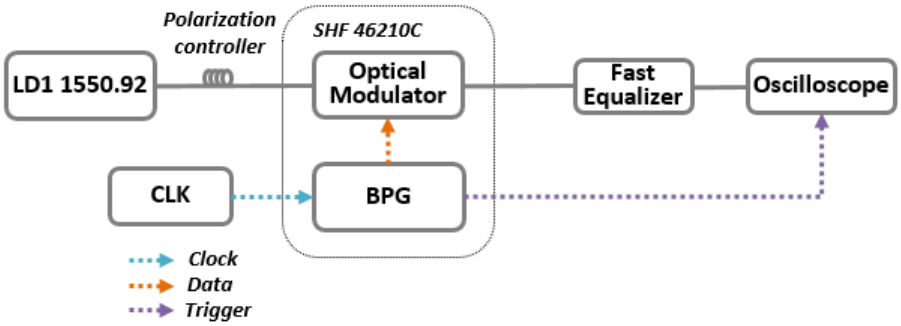


Figure 5.12: PRBS experimental set-up

The oscilloscope has to be triggered in order to scope correctly the electrical signal of the circuit. The trigger is given by the bit pattern generator (BPG) and comparing the response time between that two signals we realized that the response time was too large, out of the design. After many suppositions, the point was that the trigger signal comes out earlier than the optical signal. The reason is that inside the transmitter the MZ modulator has few meters of fiber before going to the equalizer, so that introduces a delay respect to the trigger.

Figure 5.13 shows the delay of the data respect to the trigger. The delay is 140 ns, but regarding the time scale that we are working with, the length of the cables matter. The trigger cable is one meter shorter that the data cable, it means that a one-meter propagation time of the cable has to be reckoned.

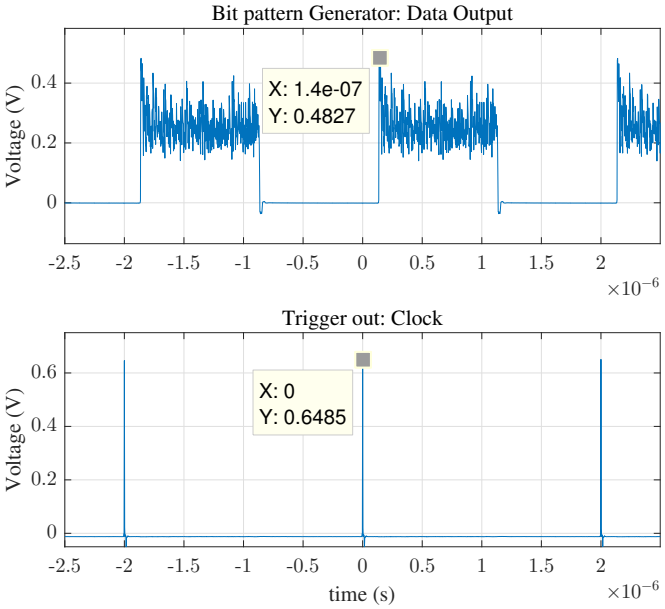
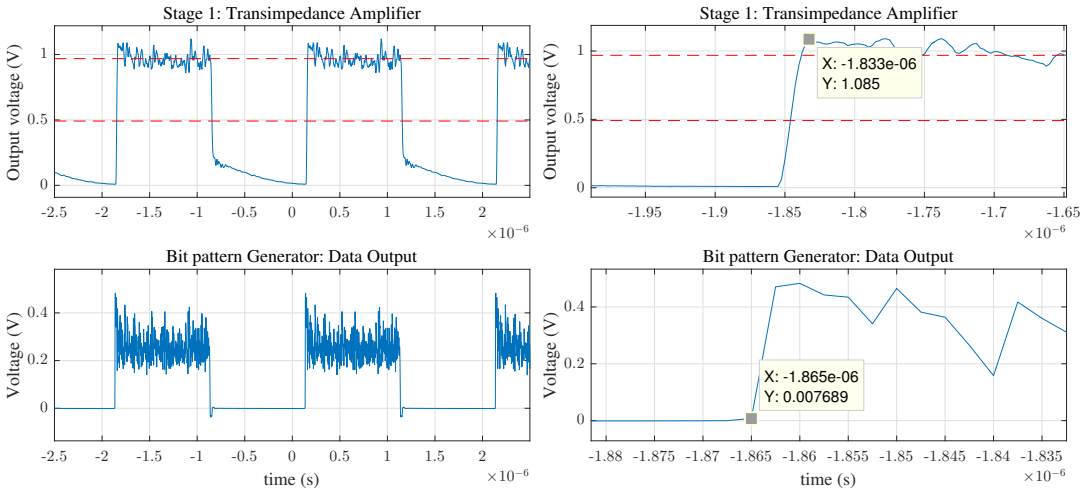


Figure 5.13: Delay time between trigger and the data output

The delay of a cable is determined by the dielectric constant of the cable. The velocity factor is the speed at which the signal propagates through a material compared to the speed of the same signal through the vacuum. In our case, a common dielectric such as teflon is tabulated and the time delay is 5 ns/m [22]. This leads to a time delay of 135ns.

The following step is to measure the response time in each stage. To make it easier, we directly plot the response time with the data instead of the trigger signal. Figure 5.14a depicts the output voltage response of the transimpedance stage. The average input power measured with the power-meter is -20dBm. Taking into account that the Pseudo Random Bit Sequence (PRBS) patter has a duty cycle of 50%, so the peak power is the double. In other words, the peak power is 3dB more than the average one, -17dBm. Checking the voltages with the DC graphs (see again Fig 5.3), the response of the circuit is the expected one.

Regarding the smoothness of the trace when the data is on, we realise that the circuit does the average value of the 10G data, thus obtaining a fluttered shape that is enhanced by changing the data rate. Concerning the response time, Figure 5.14b shows the response time of the first stage. Subtracting the two times, the delay time is 32 ns, but the one-meter difference between the fiber and the coaxial cable adds an extra time of 5 ns, so the total delay time is 37 ns. All in all, the delay is quite close to the simulation demonstrated in the previous chapter.



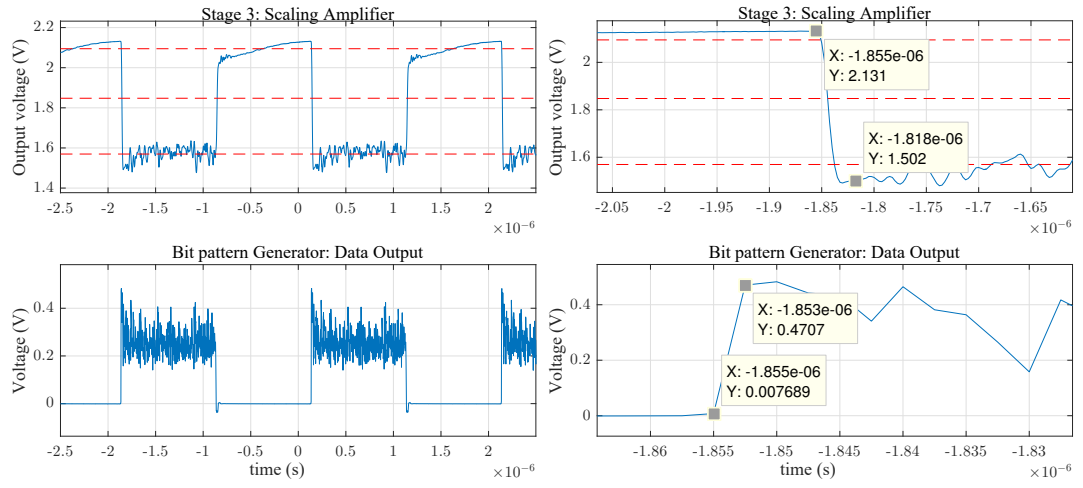
(a) General overview of the first stage, output voltage response and data output signal

(b) Zoom in of the output response, delay time

Figure 5.14: Output response of the TIA stage

The next stage is the scaling amplifier, but the IC components is the same than the previous stage. What does it mean? It means that the specifications of the component are the same, i.e the response of the circuit is constrained by the slowest IC. Then, one can expect a response time similar to the previous stage. Figure 5.15 represents the output response of the stage 2. Focusing on the right graph, the circuit scales the data voltage to the corresponding voltage that the voltage-controlled current source needs to apply an output current. The shape is the same than the previous stage, so any distortion is added (see Fig 5.15a). The left graph shows the settling time of the data, subtracting both values a time delay of 37ns and adding the extra meter difference, one can calculate a total delay time of 42 ns.

The difference between the first stage and the second one is less than 5 ns since it is the same IC but with different topology (transimpedance and inverting configuration)

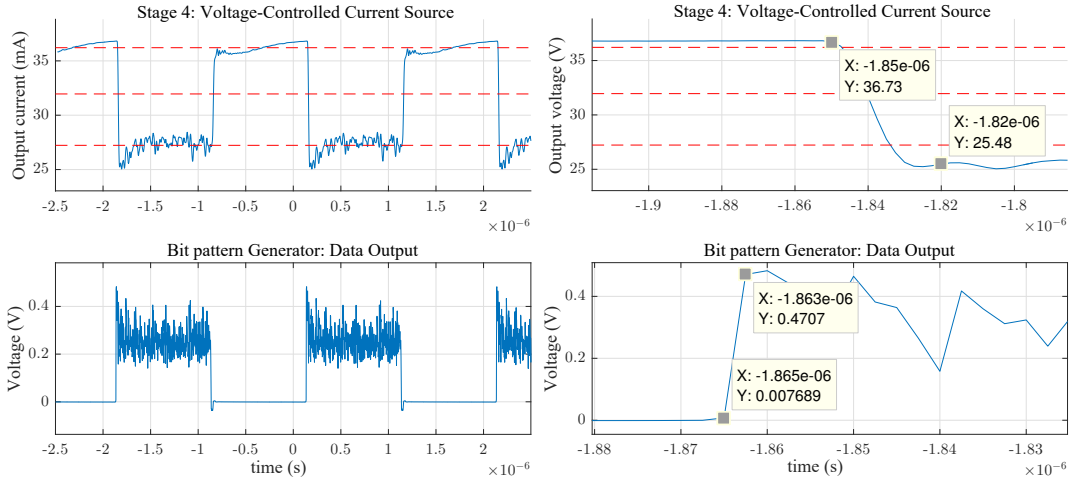


(a) General overview of the second stage, output voltage response and data output signal

(b) Zoom in of the output response, delay time

Figure 5.15: Output response of the scaling stage

Figure 5.16 is the representation of the last stage, where the input voltage is converted to output current. On one hand, Figure 5.16a shows the output current level that corresponds to the input voltage provided by the previous stage. Regarding the shape, it adds some distorting at the beginning of the trace, that overshoot is because of the roll-off compensation network and it can be improved by changing the values experimentally since the simulation does not reproduce the parasitic capacitances added by the PCB traces. On the other hand, Figure 5.16b shows the response time respect to the input data. The same as the previous cases, subtracting both times, one can obtain a settling time of 45ns. Finally, the response time of the whole circuit taking into account all the variables is 50 ns.

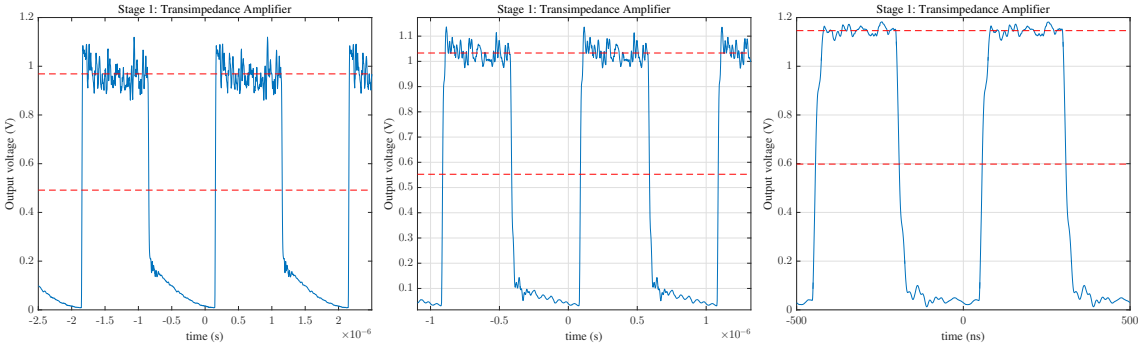


(a) General overview of the second stage, output voltage response and data output signal

(b) Zoom in of the output response, delay time

Figure 5.16: Output response of the VCCS stage

Moving towards the quality of the signal, we evaluate the circuit with different data rates: 10Gbps, 20Gbps and 40Gbps. The purpose of that experiment is to check how the data-rate affects to the response of the circuit.



(a) 10Gbps

(b) 20Gbps

(c) 40Gbps

Figure 5.17: Comparison between different data rates in the same stage

Figure 5.17 shows the different circuit responses depending on the data rate. First one should point out that the same pattern $(2^7 - 1)$ is used for all data rates. Hence, the period of the input signal decreases proportionally to the frequency, confirming that the bandwidth of the circuit is large enough to process the packets from $500ns$ to $2\mu s$. Moreover, there are clear differences

between Figure 5.17a and Figure 5.17c. 40GHz signal is smoother than the 10GHz as a result the circuit filters out better the RF signal acquiring a constant average power.

5.4 Full-Flexible circuit : UI and measurements

This second prototype is designed with a reconfigurable scaling stage. The slope and reference voltage are key parameters to fit properly the output current to the transfer function of the SOA. Moreover, the main advantage is related with the ability of remotely adapt the response of the circuit to any SOA transfer function.

5.4.1 UI - User interface design

For the purposes of the experimental measurements, two control plane applications have been implemented and deployed. Figure 5.18 represents the design which makes possible the communication between the digital pots and control master. The client is connected to the host/server via http protocol. Then, the server interacts internally with I2C protocol at the same time that I2C connects to the slaves (AD5272, AD5259).

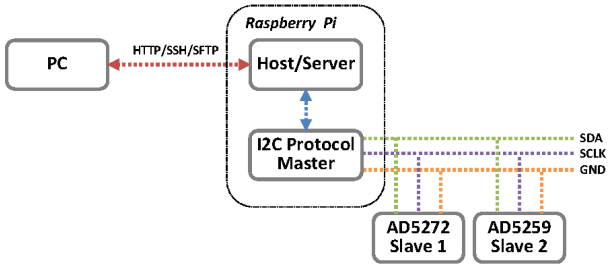


Figure 5.18: Diagram of the control plane

The user can access to the UI with any browser and dynamically set the value of the two digital potentiometers. UI is designed in such a way that can be split in three columns and each column is intended for:

1. Specific functions of each IC, calculation of the total resistance and the offset/slope.

2. Write/Store Data to the registers, for instance, AD5259 contains a EEPROM where last value stored is dumped to the register. On the contrary, AD5272 has 50-times programmable fuse blow.

3. Read Data from register or EEPROM/FUSE.

In short, Figure 5.19 illustrates the tab which controls AD5259. For the matter of debugging, the first column uses an array of 16 bits that are written directly to the register. The first eight bits are the instructions or operations of the potentiometer and the last eight bits are the value of the resistance itself. Moreover, following the equations previously explained, the total resistance and the reference voltage of the circuit is shown for each case. Once the debugging stage was finished, the two other columns were implemented. Each button just applies a different codification of the 16-bit array.

The second step was to design the digital rheostat control plane. For the AD5272/AD5274, the shift register is 16 bits wide, it consists of two unused bits, which should be set to zero, followed by four control bits and 10 data bits, and data is loaded MSB first (Bit 15). The four control bits determine the function of the software command. Figure 5.20 shows the graphic user interface for

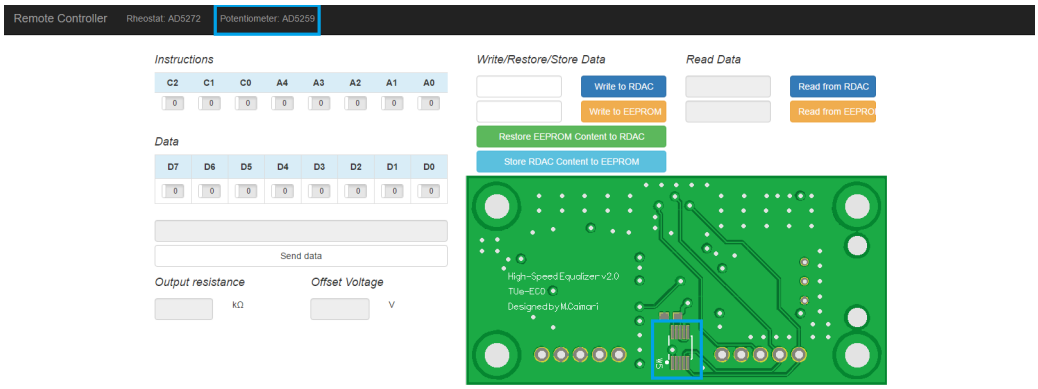


Figure 5.19: Digital potentiometer UI - AD5259

the rheostat. Being a more complex integrated circuit, first column depicts a quick commands and control register flags. Two of them, write protection and resistor performance mode, are intended for updating of wiper position through a digital interface and activating a 1% end-to-end resistor tolerance that ensures a ±1% resistor tolerance on each code. Besides, total resistance and slope are calculated and visualized in the same column. Finally, the other two columns have the same purpose as before, writing and reading the registers of the digital pot.

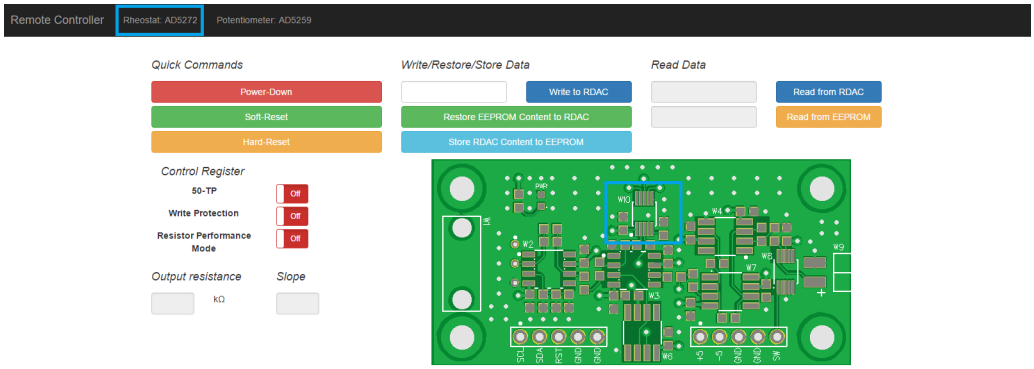


Figure 5.20: Digital rheostat UI - AD5272

5.4.2 Digital Potentiometers

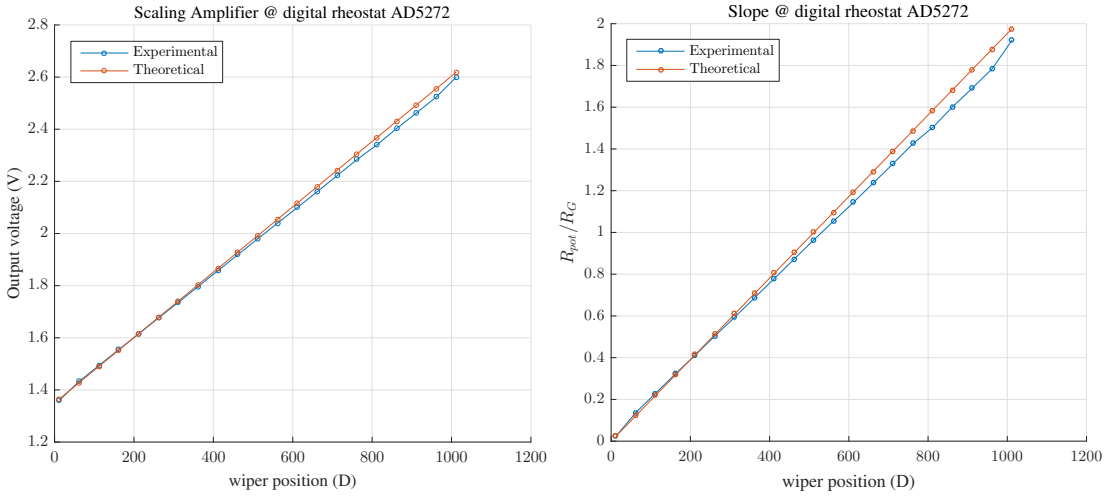
AD5272 - Slope

The general equation for determining the digitally programmed output resistance between the W terminal and A terminal is as follows:

$$R_{WA}(D) = \frac{D}{1024} \cdot R_{end} \tag{5.3}$$

where D is the decimal equivalent of the binary code loaded in the 10-/8-bit register and R_{WA} is the end-to-end resistance ($20k\Omega$).

In the experimental measurements, since the stage is soldered and functionally working, the multimeter measures the equivalent resistance measured between the two points. As a result, the measurement of the total resistance has to be done indirectly. From equation 2.30, we can obtain the value of the feedback resistance. As it is depicted in Figure 5.21, output voltage is plotted in function of the wiper position (D). A linear relationship along all the wiper positions is demonstrated. Calculating the slope of the circuit, it should take value from 0.05 up to 2 since the value of these resistances are $20k\Omega$ and $10k\Omega$.



(a) (b)

Figure 5.21: AD5272 output voltage measurement and slope calculation

AD5229 - Reference Voltage

For the reference voltage, digital potentiometer easily generates a voltage divider. In Figure 5.22 is shown such configuration. The polarity of voltage across Terminal A to Terminal B, is positive and 5V. Ignoring the effect of wiper resistance for approximation, connecting the A terminal to V_{DD} and the B terminal to ground, one can obtain a voltage divider from 0V up to 1 LSB less than 5V. In brief, the general equation which defines the output voltage of the wiper with respect to ground is:

$$V_W = \frac{D}{256} \cdot V_A + \left(\frac{256 - D}{256}\right) V_B \tag{5.4}$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Figure 5.23 represents the output voltage of the voltage divider with respect to the wiper position. Besides, the total wiper resistance is calculated as an extra measure. In total, a linear behaviour is observed for the whole range.

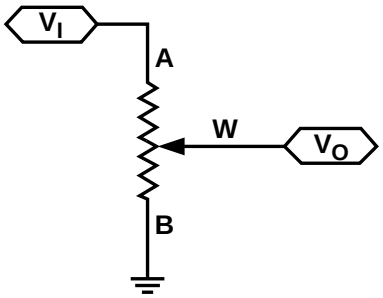
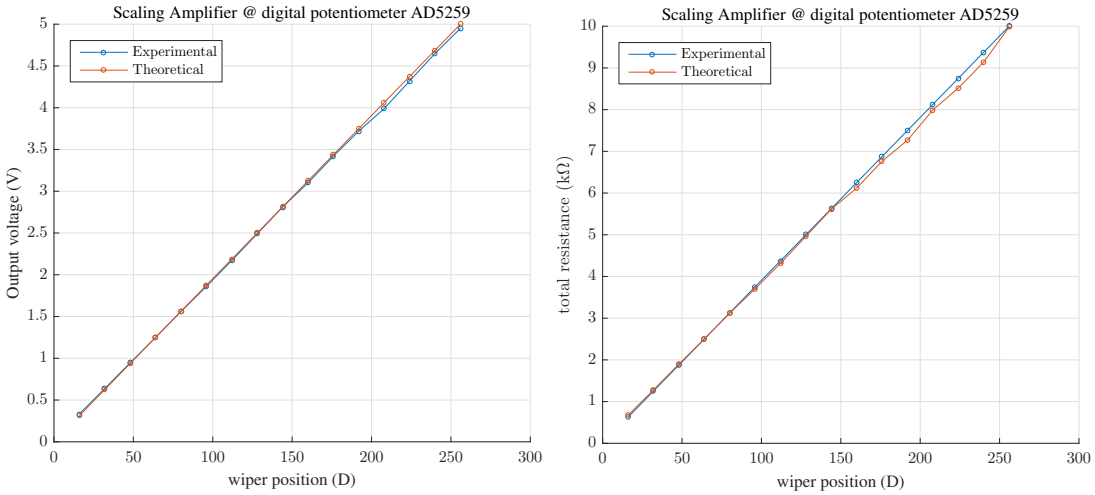


Figure 5.22: Potentiometer configuration



(a) (b)

Figure 5.23: AD5259 output voltage measurement and total resistance calculation

5.5 Timing

A network analysis tool helps us to measure the response time for the connection establishment between the PC and the device. The three main time breakdown phases are explained as follows:

- *Request sent.* The request is being sent.
- *Waiting (TTFB).* The browser is waiting for the first byte of a response. TTFB stands for Time To First Byte.
- *Content Download.* The browser is receiving the response.

The waiting time (TTFB) is the time that the host takes to send the values through the I2C protocol and reconfigure the slope or reference voltage with the digital potentiometers. Table 5.3 and 5.2 presents the total time spent for a read/write command request. Focusing on that time, for both cases only takes 68 ms to reach the digital potentiometer and setup the correct value from the browser. Nonetheless, the response is shown to the client in 110 ms and 118 ms for read and write command respectively.

Moving towards an upper layer, recently our research group has presented a final demonstration of a 4x4 fast optical switch prototype. A software defined networking provisioning and virtualizing a control interface for a fast optical switch has been developed [23].

Table 5.2: Read Command

Request/Response	time (ms)
Request sent	0.17
Waiting (TTFB)	68.86
Content Download	110.76
Total	181.82

Table 5.3: Write Command

Request/Response	time (ms)
Request sent	0.16
Waiting (TTFB)	68.87
Content Download	118.51
Total	191.96

In this context, for a OPS connection establishment, it takes around 420 ms for the configuration. Therefore, the reconfigurability of our design fits in the time scale for a demanding SDN-based programmability.

5.6 Summary

The characterisation of the prototypes has been presented in this chapter. Starting from the operating point analysis up to testing PRBS packet-base data. Based on the DC analysis, the measurements are compared with simulations and ideal mathematical model. Each stage behaves as were predicted except for the logarithmic amplifier. SPICE model saturates at 1V input voltage while the practical model saturates at 3V, increasing quite the dynamic range of the stage. The transimpedance amplifier behaved linearly for a range of -40dBm up to 12dBm (28dB dynamic rage). The scaling amplifier and voltage-controlled current source, both of them thoroughly follow simulation results.

The experimental results confirmed the dynamic switching of the circuit was less than 100ns. On the contrary of the simulations results, the slowest rising time is set by the full-flexible configuration (60 ns). This is because the simulation was performed with a theoretical value of the parasitic capacitance, so giving an approximate value. Moreover, the slowest settling time is measured in the last stage, but still in the specifications, 100ns. Being analog circuit, the lowest stage limits the total time operation of the circuit.

The capability of handling different data-rate with 10Gbps, 20Gbps, 40Gbps is analysed. The circuit presents a ripple in the signal which is not completely filter out since the bandwidth of the circuit, even the photodiode is not low enough. The flattest response is logically achieved by a 40 Gbps.

The reconfigurability of the prototype has been demonstrated. Digital pots controlled via I2C protocol are included in the scaling stage. By designing a property interface, the slope and reference voltage of this stage scaling amplifier can be set in advance, adapting the circuit to different transfer functions of the circuit. Regarding the total response time, it takes 68 ms as an average value to reconfigure the equalizer.

Chapter 6

Optical experimental setup

In this chapter, a first proof of equalization is presented. To this purpose, SOA characterisation is required in order to accurately dimension the slope and reference voltage of our circuit, it is presented in section 6.1. Once the transfer function is known, experimentals results including two different optical setups are presented in section 6.2. Finally, the full circuit includes the logarithmic stage and the High-Speed Equalizer v2.0, experimental results showing the reconfigurability and equalization are reported in section 6.3.

6.1 SOA Characterisation

Before starting with the equalization of the packets, one have to ensure which type of SOA is working with and full characterise it beforehand. The most critical parameter of an optical amplifier in many applications such ours is its gain. SOAs might show a promising result as in-line amplifiers making suitable for metropolitan (short-region) and access networks, where the less performance amplifiers are tolerated (e.g high noise figure).

6.1.1 SOA Gain

Figure 6.1 depicts the experimental setup used to characterise the SOA[1]. The laser is injected into the SOA with a polarisation controller corresponding to the maximum SOA gain.

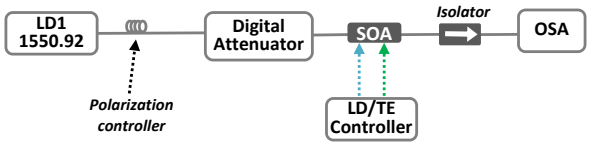
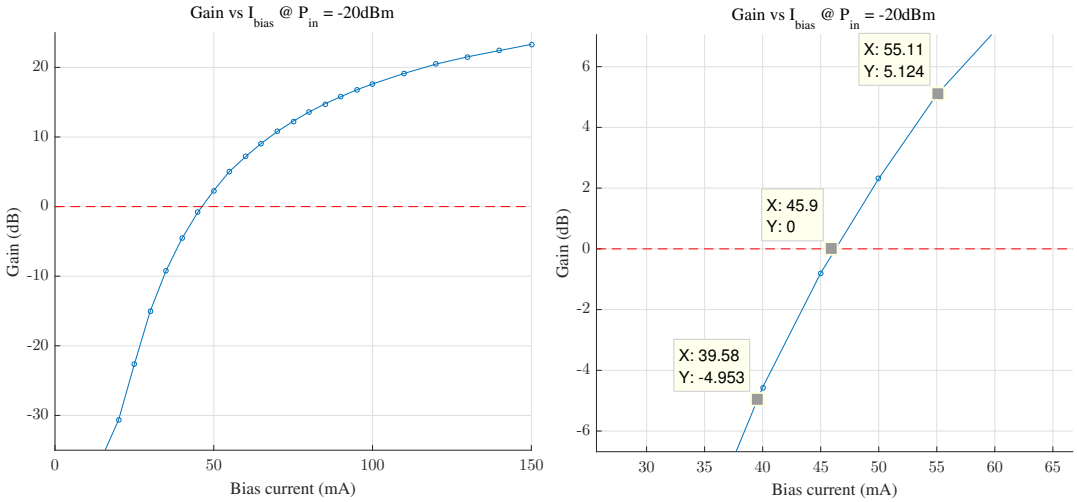


Figure 6.1: Experimental set-up

First, the gain versus the bias current is measured. To do that, the current of the controller is changing meanwhile the input power is kept in a certain value, in our case, at -20dBm. Another consideration to proceed correctly, the temperature of the SOA has to be constant and it was set to 25 degrees, all the increasing and decreasing of the current must be done carefully. As depicted in the Figure 6.2, the gain increases dramatically until reach the transparency point of 0dB at 45.9 mA. After such point, the gain grows gradually reaching a peak of 23 dB at a high current of 150mA. Ideally we want a straight line in a range of 10dB, Figure 6.2b shows a good approximation where that dynamic range is achieved by attenuating the highest power packets

[1]Manufacturer: JD Uniphase, Serial No. 899, Type: CQF872/108C

and amplifying the lowest ones. The values provided by the equalizer should be in the range of 40 mA up to 55 mA.



(a) Measured gain vs bias current

(b) Zoom in a range of 10dB

Figure 6.2: SOA gain vs bias current curves

6.1.2 Small signal gain

Small signal gain usually makes reference to the highest gain of the optical amplifier since it is achieved when the input signal power does not saturate the SOA. Figure 6.3 shows the small signal gain, when the gain is dropped 3 dB respect to its small signal gain, the output power is called output saturation power. The relative input power is called input saturation power. In our case, the SOA saturates when the output power reaches a value around -2.5dB.

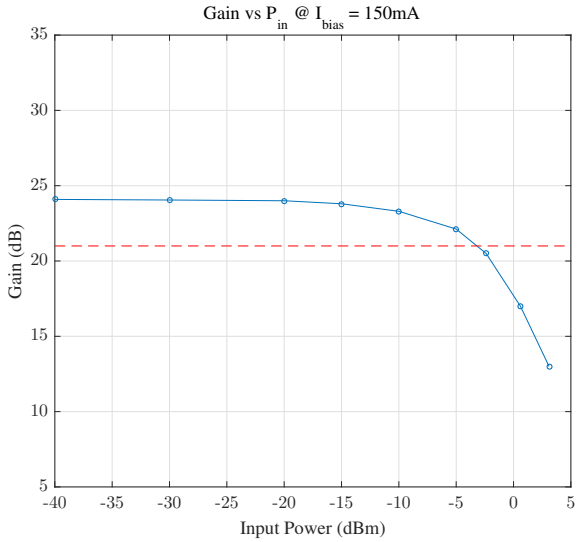


Figure 6.3: Small signal gain, measured gain vs output power

6.1.3 Resistance

The last parameter important for our purpose is the dynamic resistance of the SOA. As it is explained in the chapter 3, the VCCS is independent of the load up to certain value as well as the stability of the circuit. Knowing the value of the SOA resistance helps to re-design the last stage of the circuit to optimize the rising/falling time and the quality itself. Figure 6.4 depicts a maximum resistance of 80Ω at 20 mA and it decreases as long as the bias current is increasing, with a resistance of 25Ω at 70mA. The dynamic resistance of the SOA allows us dimension the series resistance to stabilize the circuit without limiting the maximum achievable bias current.

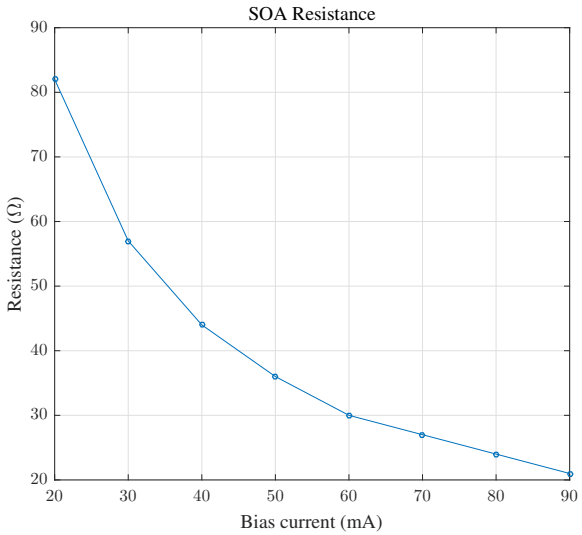


Figure 6.4: Calculated resistance vs bias current

6.2 Power Equalization: High Speed Equalizer v1.0

For these first experiments, fixed-slope configuration is used without logarithmic stage, only the reference voltage is variable. As a consequence, simply two points of the whole range can be equalized (recalling in section 2.1).

6.2.1 PRBS packets-based experimental setup

The packets are generated with a packet-based pattern. By changing the power of the laser the output power of the optical transmitter is changed proportionally. So, the first case occurs with an input power of -3dBm and the another for -13dBm (10 dB difference).

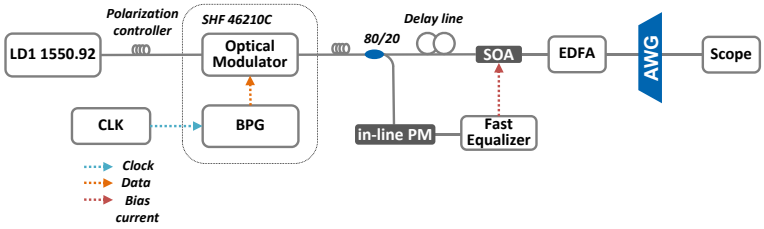
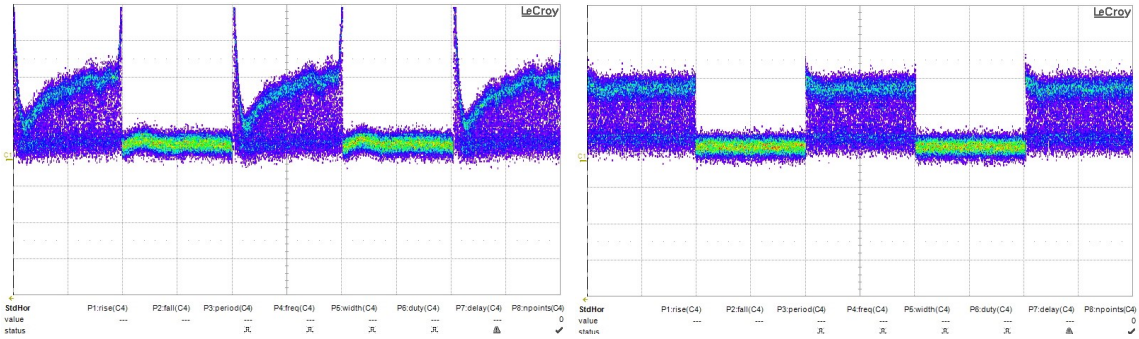


Figure 6.5: Experimental set-up for PRBS test

The equalizer provides the bias current to attenuate the first case by 5dB and to amplify the second one by 5dB. Figure 6.6 represents the output of the SOA for the two input powers. When the highest power is attenuated 5dB, the beginning and end of the packets are not equalized due to the rising time of the circuit. Moreover, the last stage is not well tuned causing an undershoot to the signal (see Figure 6.6a). Amplifying by 5dB the lowest power produces a cleaner response since the circuit is almost saturated proving a constant bias current.



(a) Input power : -3dBm, output SOA equalization - 1mW/div - y axe 500ns/div - x axe

(b) Input power : -13dBm, output SOA equalization - 1mW/div - y axe 500ns/div - x axe

Figure 6.6: Two point equalization in 10 dB packet difference

Finally, Table 6.1 shows the key values used in this experimental setup. The voltage-controlled current source has to be tuned, by changing the series resistance and the feedback capacitance the response of the signal can be properly modified.

Table 6.1: Components value of equalizer

	R_F	R_G	R_{sense}	R_{series}	R_{loop}	C_c
TIA	49.9kΩ					
Scaling Amplifier	84Ω	100Ω				
VCCS			3Ω	40Ω	2kΩ	$30pF$
$V_{REF} = 1.83V$						

6.2.2 External analog MZ modulator setup

This third setup includes a new element: external MZ modulator[2], shown in Figure 6.7. The main advantage to respect with the previous one is the possibility to generate two power levels of a continuous PRBS sequence. Two polarization controllers are placed to achieve the maximum power at the output of each modulator. The external modulator is controlled by a bias power supply and a function generator, with an extinction ratio up to 20dB. Properly setting the bias and RF signal, a total of 10 dB difference between the two levels is reached.

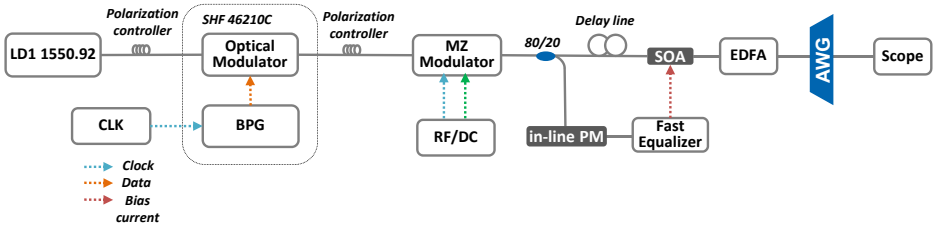
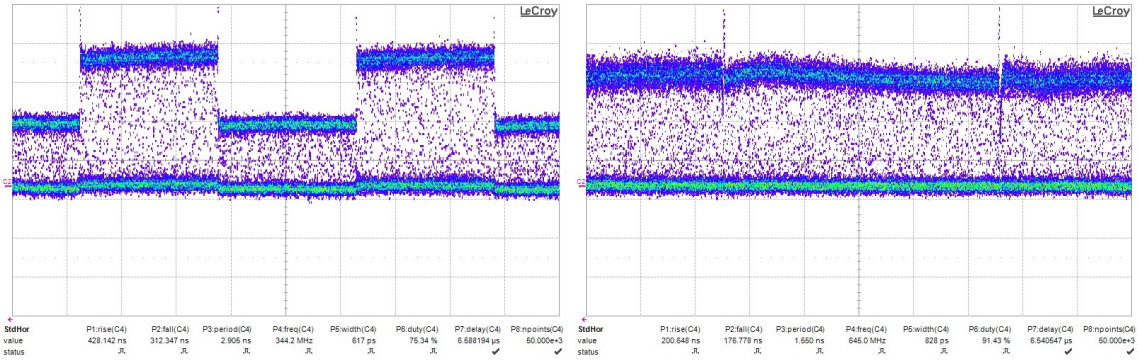


Figure 6.7: External MZ modulator setup

Figure 6.8a shows a completely two power levels at the input of the SOA. Again, following the same principle as before, the highest power is attenuated by 5dB and the lowest power amplified by 5dB. The results of the equalization are shown in Figure 6.8b. The undershoot is completely removed and the rising time is decreased as a result.



(a) Input packets into SOA - 1mW/div - y axe 1u/div - x axe

(b) Output SOA, equalization - 1mW/div - y axe 1u/div - x axe

Figure 6.8: Second proof of equalization, 10 dB dynamic range - two points.

In brief, Table 6.2 shows the key values of the equalizer. After the optimization of last stage, the roll-off and series resistance by 47pF-2kΩ and $R_L = 30\Omega$ were replaced.

[2]Manufacturer: JDSU, Serial No. 44061G

Table 6.2: Components value of equalizer

	R_F	R_G	R_{sense}	R_{series}	R_{loop}	C_c
TIA	49.9kΩ					
Scaling Amplifier	83Ω	100Ω				
VCCS			3Ω	30Ω	2kΩ	$47pF$
$V_{REF} = 1.83V$						

To sum up, these two set-up has helped us to fully understand the optical part. The first proof of equalization starts in the next section since up to now only two point were able to be equalized.

6.3 Power Equalization: High Speed Equalizer v2.0 + Log Stage

In this section, the experiments are performed with the full-flexible configuration and the addition of the logarithmic stage. Firstly, proofing the equalization for a continuous mode is crucial to check the functionality of the device. Secondly, the response time is measured in each stage and at the output of the circuit, showing which is the most restrictive stage.

Table 6.3: Wiper position of the digital potentiometers

	First Region (-5dBm to 5dBm)	Second Region (0 dBm to 10dBm)
Rheostat (wiper position D)	460 (8.3kΩ)	520 (10.5kΩ)
Potentiometer (wiper position D)	90 (1.85V)	102 (2.02V)

By using the User Interface (UI) described in the previous chapter, the slope and reference voltage are set according to two different operating regions (see Table 6.3).

6.3.1 Continuous mode

Figure 6.9 represents the experimental set-up used for the first proof of equalization. After the digital attenuator, a polarization controller is placed to achieve the maximum gain of the SOA. Followed by a coupler the power is transferred into two paths and monitored before entering to the equalizer. A delay line is added to synchronise the signal between the two paths. Finally, an optical spectrum analyser measures the power at the output of the SOA.

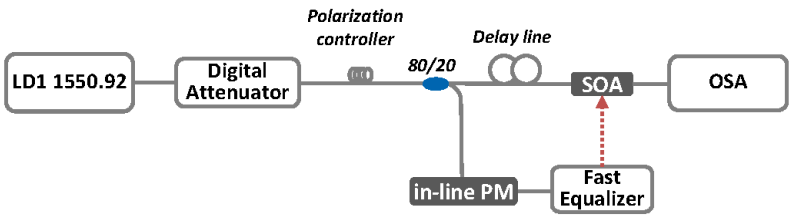
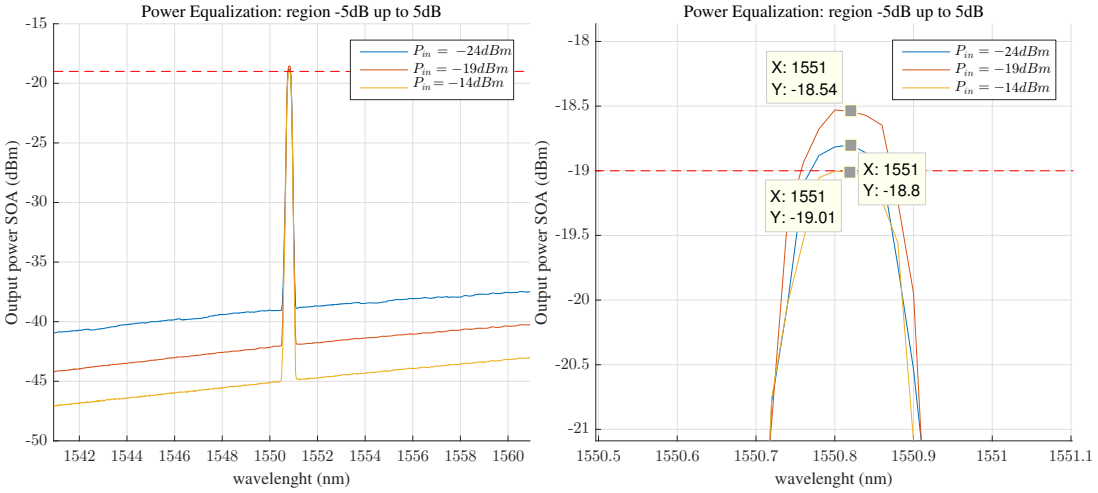


Figure 6.9: Continuous mode

Recalling Figure 6.2b, the first region where the equalizer works is between -5dB and 5dB. This is one of the most linear region of the SOA transfer function. In this case, the highest power is attenuated by 5dB and the lowest power is amplified by 5dB, achieving a total dynamic range of 10dB.

To do so, the slope and reference voltage are reconfigured in order to provide the correct amount of current to the optical amplifier. In this first region, three points are equalized in a range of 10dB difference. The input power starts at -14dBm up to -24dBm, stopping in a middle range of -19dBm. The circuit changes the output current automatically as long as the input power is changing. In the table 6.4, the values are summarised showing an equalization for a 10dB input power range.



(a) SOA output power for a first region

(b) Zoom-in, first region

Figure 6.10: Power equalization: first region

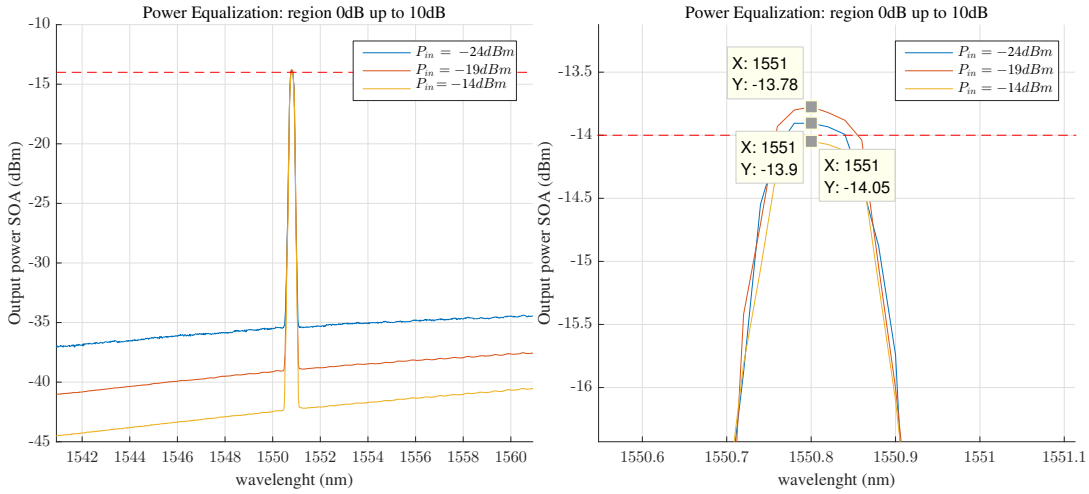
Table 6.4: First region: -5dB up to 5dB

P_{in}	V_{in} - Scaling Stage	I_{out} - VCCS	P_{out}
-14dBm	1.20 V	40mA	-19.5dBm
-19dBm	1.43 V	47.6mA	-18.8dBm
-24dBm	1.67 V	55mA	-19.0dBm

To exploit the reconfigurability of the second prototype, a second region of the SOA is explored. It goes from 0dB up to 10dB, attenuating any power (see Table 6.5). The two extremes of the range are well tracked, otherwise the middle point has an error differing from the reference value in 0.22 dB (see Figure 6.11b).

Table 6.5: Second region: 0dB up to 10dB

P_{in}	V_{in} - Scaling Stage	I_{out} - VCCS	P_{out}
-14dBm	2.08 V	47.6mA	-13.9dBm
-19dBm	1.76 V	59mA	-13.78dBm
-24dBm	1.38 V	65mA	-14.05dBm



(a) SOA output power for a second region

(b) Zoom-in, first region

Figure 6.11: Power equalization: second region

OSNR

A quick analysis about the Optical Signal to Noise Ratio (OSNR) is presented in this section. OSNR is the measure of the ratio of signal power to noise power in an optical channel. From the static curves of the continuous mode, one can calculate it for the two different regions. The optical noise power increases proportionally to the increasing of the bias current. Attenuating the signal provokes an output power low enough to be reflected in the OSNR (see Table 6.6). Even though the optical noise power is higher in the second region, OSNR is better since the optical signal power is much higher than the first region (see Table 6.7).

Table 6.6: First region: -5dB up to 5dB

	Optical Noise Power (dBm)	Optical Signal Power (dBm)	OSNR (dB)
P_{min}	-37.5	-18.8	18.7
P_{mid}	-40.23	-18.54	21.69
P_{max}	-43.02	-19.01	24.01

Table 6.7: Second region: 0dB up to 10dB

	Optical Noise Power (dBm)	Optical Signal Power (dBm)	OSNR (dB)
P_{min}	-34.45	-13.9	20.55
P_{mid}	-37.56	-14.05	23.51
P_{max}	-40.51	-13.78	26.73

6.3.2 Switching mode

This experiment is intended to show the dynamics of the equalization. An external analog Mach-Zehnder modulator is placed after the data modulator to generate two different power levels. By changing the bias point and the RF signal, the period and the power level can be set. Moreover, at the output of the SOA an EDFA and AWG are introduced to amplify and filter the signal to correctly visualise it with an optical oscilloscope.

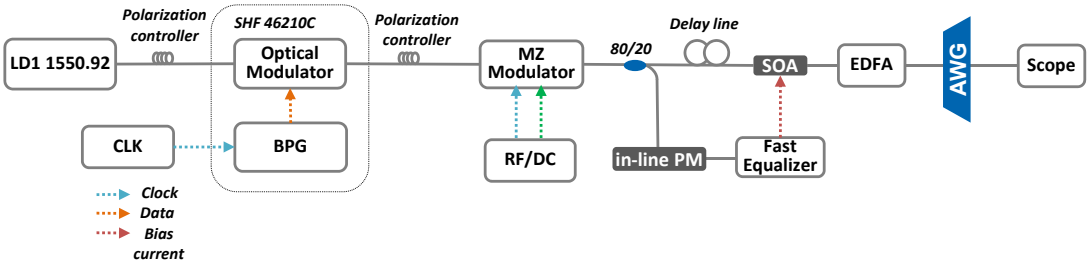
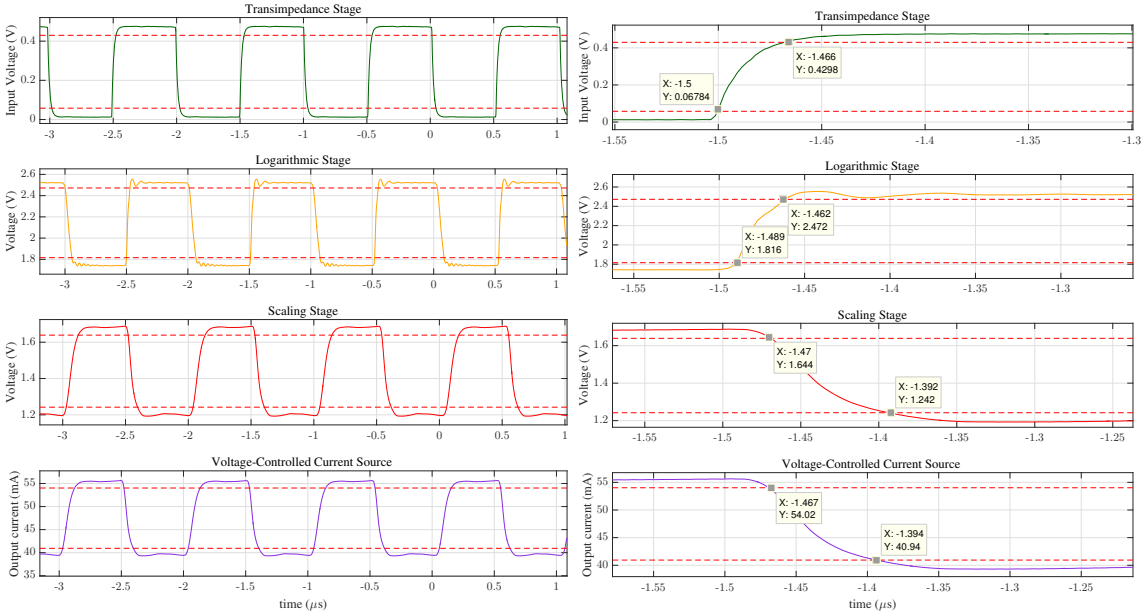


Figure 6.12: Switching mode, experimental setup to measure the transient time

The electronic traces of each stage are shown in Figure 6.13 and summarized in table 6.8. Zoom in the signals, one can observe that the stage which takes longer to reach the final value is the scaling amplifier. A total of 150 ns is the response time of the circuit, slightly higher than the simulated (see Figure 6.13b). The output of SOA is presented in Figure 6.14, working directly with the payload shows that is necessary to feed the optical power of the packet in advance. Otherwise, the time that the circuit takes to change the two power levels is transmitted to the payload. Figure 6.14b shows that the first and last region of the payload are affected by this transient time, but the rest of the payload is equalized.

Table 6.8: Rising and settling time per stages

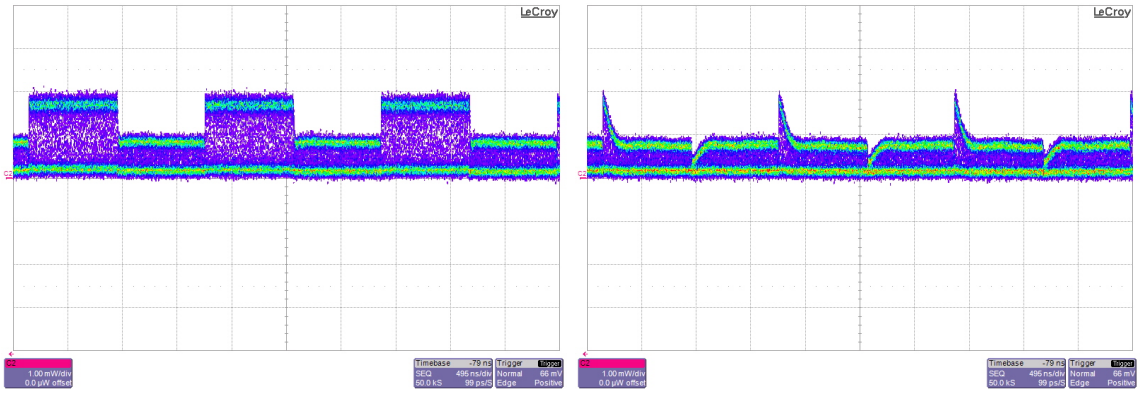
	TIA	LOG	Scaling Amp	VCCS
t_r	42ns	40ns	72ns	75 ns
t_s	60ns	70ns	150ns	150ns



(a) Electronic signals at each stage

(b) Zoom in, electronic signals at each stage

Figure 6.13: Response time



(a) input packets to SOA, 1mW/div - y axe 500ns/div - x axe

(b) Equalization, output of SOA, 1mW/div - y axe 500ns/-div - x axe

Figure 6.14: Optical traces at the input/output of the SOA

6.4 Summary

A proof of equalization has been presented in this chapter. The SOA has been characterised, including the gain in function of the current, small signal gain and dynamic resistance. A linear region of the transfer function between -5dB and 5dB has been chosen as operation region. The circuit has to provide current between 40 mA to 55mA. A power equalization setup with the fixed-slope configuration and without logarithmic amplifier has been analysed, showing three different experimental setup and equalizing two power level with 10 dB difference. After adjusting the last stage, a full range of power equalization has been demonstrated. By using the full-flexible prototype and adding the logarithmic stage, a input power dynamic range of 10 dB has been achieved, equalizing the full range. Moreover, exploiting the reconfigurability of the prototype, two regions of the SOA transfer function has been chosen and equalized with 0.2 dB and 0.5 dB deviation for each case. Finally, a response time of 150 ns is measured, the bottleneck comes from the digital potentiometers, the parasitic capacitances with the high value of the resistance provoke a low-pass filter with a high constant-time.

Chapter 7

Summary and outlook

7.1 Summary

To conciliate the increasing demand of the bandwidth in the data-centers, architectural and technological innovations are investigated. In our case, fast optical switching technology has been investigated along these years, finding out different issues to deal with. Several power equalization methods based on control feedback loops do not solve satisfactory the dynamic performance of the next generation of optical switch. The motivation of this master thesis was to design and implement a low-cost fast-per-packet power equalizer for an optical cross-connected switch.

Encouraging results have been demonstrated by means of simulation and experimental assessments. In short, the achievements made in this work were started from an exhausting mathematical model of the equalization problem. Describing mathematically the output response of each stage, it was determined the main structure of the circuit:

1. Transimpedance amplifier
2. Logarithmic amplifier
3. Scaling amplifier
4. Voltage-controlled current source.

Component selection and simulation have been principal and key aspect to investigate the overall behaviour of the circuit. Three main simulations has been performed: DC, AC and transient analysis. After facing the main issues of each stage, such us stability and operating point, the simulation of the full circuit has been demonstrated in two different prototypes. Simulation results indicate a response time of 100 ns for the whole circuit, where the logarithmic stage is the bottleneck imposing the slowest settling time. A power consumption of 1W has been countered for the design, which could be maintained even when handling higher output current.

PCB layout design is implemented for a total of three different prototypes: fixed-slope (High-Speed Equalizer v1.0), full-flexible (High-Speed Equalizer v2.0) and VCCS drivers (Tunable Laser Driver 1.0v). Unfortunately, the logarithmic stage was implemented in a bread-board for a fault of the design in beginning. The design of the PCB was made in a 4-layers stack-up allowing a clear and compact design. Thus, the board size of the three prototypes is 5.5cm x 8.7cm, reducing even more the cost of the PCB.

Testing and verification of the design was the next step to ensure that the circuit behaves as simulated. Based on DC analysis, the measurements are compared with the simulations and the mathematical model. The first stage, transimpedance amplifier, achieves a dynamic range of 28dB, from -40dBm up to -12dBm, enough for a total of 10 dB dynamic range of the SOA. For the log-amplifier, the simulation differs from the practical measurements. SPICE model saturates at 1V input voltage while the practical model saturates at 3V, not limiting the range of the first stage. The scaling amplifier and VCCS both steady-state behaviour fully follows the simulations.

The experimental results confirmed the rising time of the circuit was less than 100ns except for the full-flexible configuration. Being analog circuit, the lowest stage limits the total time operation of the circuit. The capability of handling different data-rate with 10Gb/s, 20Gb/s, 40Gb/s is analysed. The circuit presents a ripple in the signal, it is not completely filter out since the bandwidth of the circuit, even the photodiode is not low enough. The flattest response is achieved logically by a 40 Gb/s.

The reconfigurability of the prototype have been demonstrated. Digital pots controlled via I2C protocol are included in the scaling stage. By designing a property interface, the slope and reference voltage of this stage scaling amplifier can be set in advance, adapting the circuit to different transfer functions of the circuit. Assessment results show a connection time server-to-equalizer of 68 ms, demonstrating that the reconfigurability fits in the time scale of a demanding SDN-based environment .

In the optical experimental set-up, several preliminary results has been analysed. Learning each time that the results were not as expected. Finally, the best option to generate two optical power levels is an external analog Mach-Zender modulator. A continuous PRBS sequence is modulated into different power levels. A clear and flat signal has been achieved allowing us to proof a dynamic range of 10 dB. To do so, the final prototype including the logarithmic stage is implemented. Two main experiments has been proposed as a proof of equalization: continuous mode and switching mode. A power range between -14dBm up to -24dBm including a middle point -19dBm is used as input signal. The output power of the SOA has kept a constant value for all that range. Moreover, taking advantage from the reconfigurability two regions has been demonstrated. A first region of the transfer function is chosen, between -5dB and 5dB gain, obtaining a total of 10dB dynamic range. The output power is kept into -19dBm having a maximum difference of 0.5dB for those three points. Additionally, a second region is also chosen between 0 and 10 dB gain, no attenuation. In this case, the output power is kept into -14dBm with a penalty of 0.22 dB. Regarding the switching mode, the setup mentioned before is used to generate two power levels. A 10dB difference between the two levels is fed into the circuit. The response time is measured in each stage and at the end of the circuit. In short, the scaling stage determines the total response time of the circuit with a total of 150 ns. The equalization is correctly achieved aside from the boundaries of the packets, directly working with the payload produces this effect since the rising time of an optical signal compared to the electronic one is much faster.

7.2 Future Outlooks

A fast automatic power equalizer with 10dB dynamic range has been studied in this thesis. Promising results towards the speed and flexibility capabilities have been shown with different prototypes. Due to time limitation imposed by the framework of the thesis, it is only the first stage of the design, extra effort on optimizing and integrating all the elements is necessary for a final goal: real data center environment. In the following, some near-term improvements are proposed:

Re-design of PCB Layout

A new PCB layout is necessary if one wants to ensure the functionality of the circuit much longer. The logarithmic stage is attached with two wrapping cables, and it is soldered in a bread-board. So, the new PCB layout contemplates this extra stage. Additionally, a lot of time was dedicated to find a solution to connect the SOA and the equalizer (see Appendix D.1a), this connection became problematic causing instabilities on the circuit. A SOA socket included in the PCB is another possible solution.

Real environment experiments

All experimental set-ups were using the SHF rack and working directly with the payload. A more complex setup is essential by using external control boards, such as label extractor and FPGA to fully equalize properly the payload.

FPGA integration

The full-flexible prototype was controlled via I2C protocol using the raspberry as a control-plane. Migration of the code to a FPGA would be the next step to have all the operations in the same device.

Photonic integrated fast optical switch

Using a photonic integrated 4x4 WDM fast optical switch to exploit more functionalities of the equalizer. More than 100 components including SOAs, AWGs and couplers are integrated in the same chip. For our purposes, the photodiode would be substituted for an inner SOA of the PIC and use it to measure the input optical power. By implementing different equalizers, multiple channels could be equalized with the proper setup.

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List of Figures

List of Tables

Acronyms

AWG Arrayed Waveguide Grating. 5

COM Common-Mode Output. 27

DAC Digital Analog Converter. 7

DC Direct Current. 51–53, 59, 66, 84

DC Data Center. 2, 3

EDFA Erbium doped fiber amplifier. 5

FBG Fiber Bragg grating. 6

FPGA Field-Programmable Gate Array. 6, 7, 47, 78, 79, 87

IC Integrated Circuit. 27, 45

MEMS MicroElectroMechanical Systems. 2, 3

MZ MachZehnder. 58

O/E/O Optical-to-Electrical-to-Optical. 3

OADM Optical Add Drop Multiplexer. 2, 3, 83

OLS Optical Label Switched. 5

OPS Optical Packet Switch. 3, 4, 83

OSNR Optical Signal to Noise Ratio. 74

PCB Printed Circuit Board. 2, 7, 43–50

PIC Photonic Integrated Circuit. 79

PRBS Pseudo Random Bit Sequence. 51, 58, 59, 66

QFN Quad-FLat No-leads. 44

RF Radio Frequency. 6, 27, 41

SDN Software Defined Networking. 78

SMD Surface Mount Device. 45, 47, 49, 56

SOA Semicondutor Optical Amplifier. 4, 7

SOIC Small Outline Integrated Circuit. 44

SPICE Simulation Program with Integrated Circuit Emphasis. 23, 30, 33

TIA Trasimpedance Amplifier. 27, 83

TTFB Time To First Byte. 65

UI User Interface. 62, 63, 72, 84

VCCS Voltage-Controlled Current Source. 35, 43, 50, 77

VLSI Very Large Scale Integration. 1

WDM Wavelength Division Multiplexing. 2, 3

Appendices

Appendix A

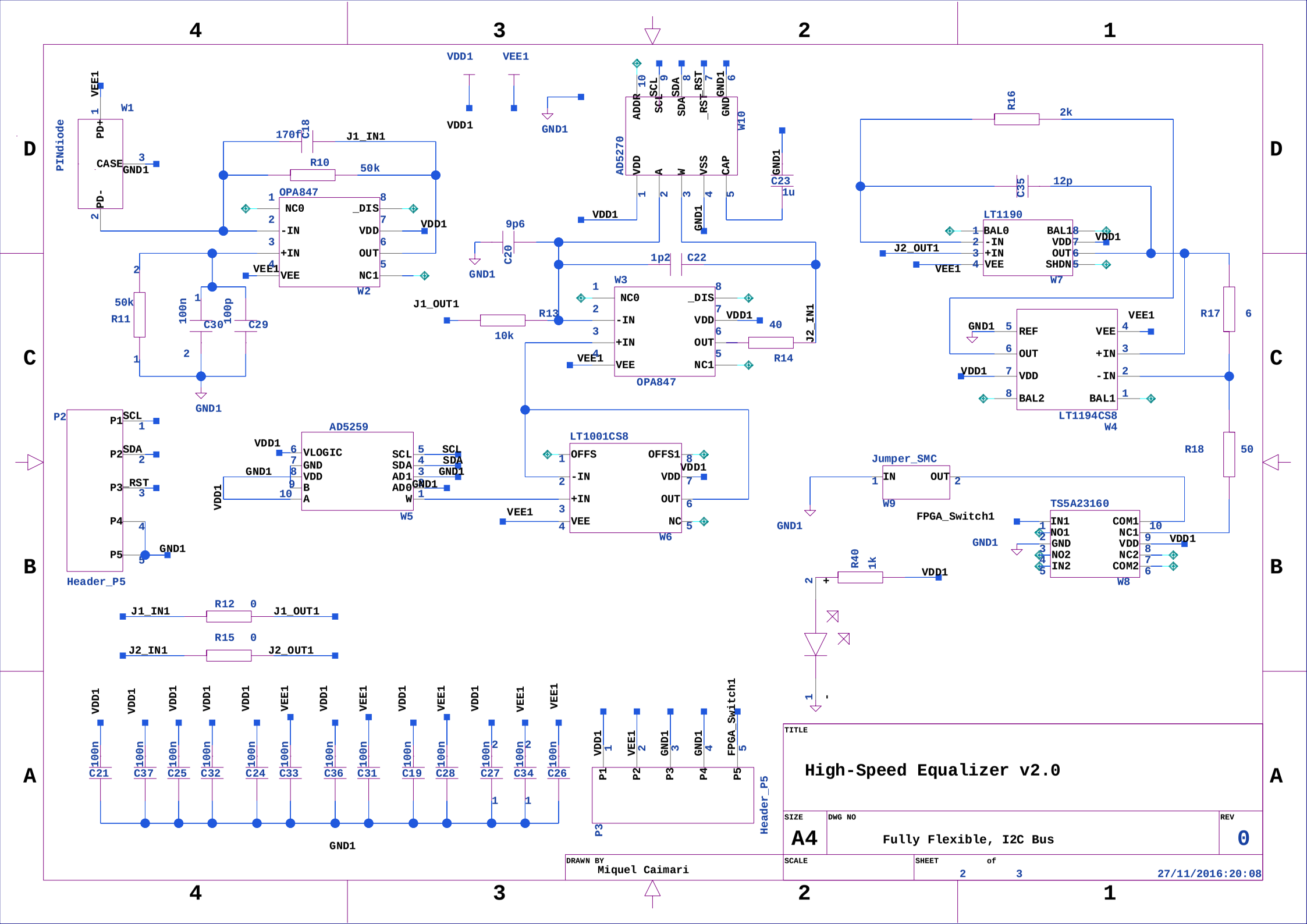
Component values: Simulation

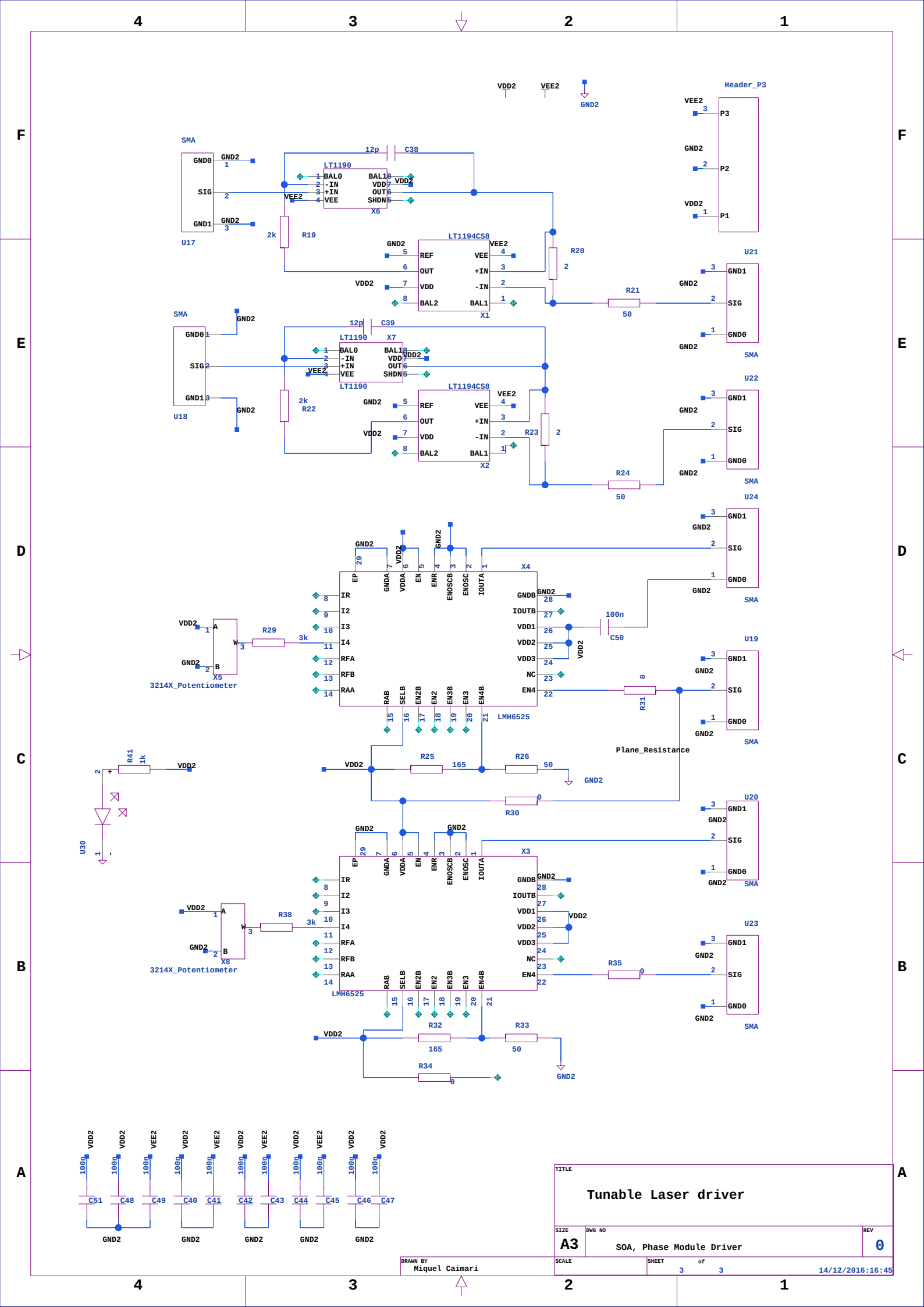
Table A.1: Components value of the full circuit

Ref.	Description
C1	capacitor, 100nF
C2	capacitor, 100pF
C3	capacitor, 1pF
C5	capacitor, 4.2pF
C6	capacitor, 200fF
C7	capacitor, 90pF
C8	capacitor, 40pF
C10	capacitor, 60pF
C12	capacitor, 60pF
Cc1	capacitor, 0F
D1	diode
Load1	resistor, 0
R1	resistor, 49.9K, 1%
R2	resistor, 10K, 1%
R3	resistor, 8.3K, 1%
R4	resistor, 49.9K, 1%
R5	resistor, 10K
R6	resistor, 800m
R7	resistor, 10K
R8	resistor, 499
R9	resistor, 499
R10	resistor, 499
R11	resistor, 500
R12	resistor, 3.01K
R13	resistor, 1.87K
Rc1	resistor, 0, 1%
Sense1	resistor, 0, 1%
OPA847_Model	Texas Instrument
LT1190	Linear Technology
OPA847_Model	Texas Instrument
LT1194	Linear Technology
ad8138	Analog Devices
AD8310	Analog Devices

Appendix B

Schematic entry

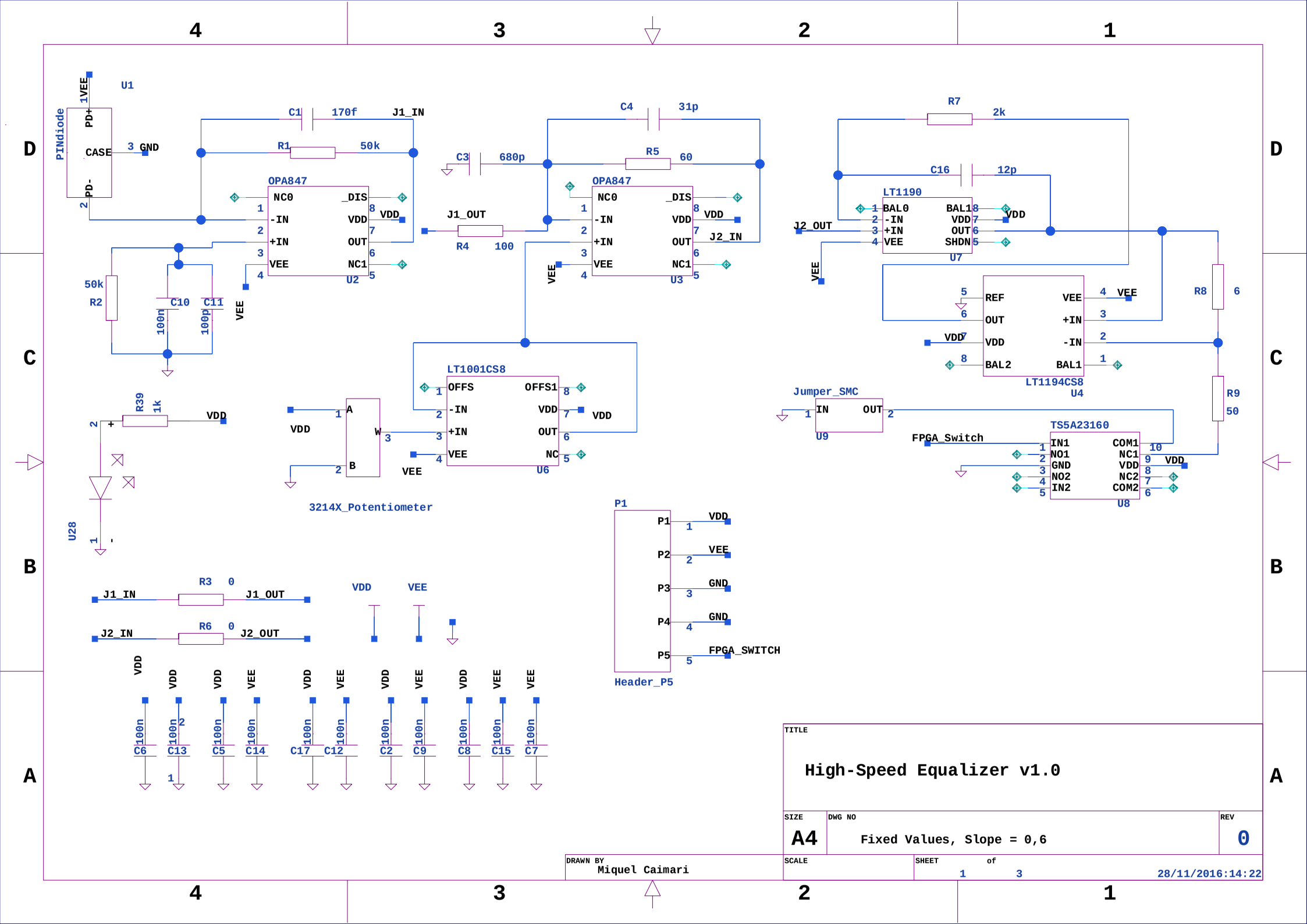

High-Speed Equalizer v2.0
Fully Flexible, I2C Bus
Miquel Caimari
A4
0
27/11/2016:20:08
OPA847
AD5270
LT1190
LT1194CS8
AD5259
LT1001CS8
TS5A23160
Jumper_SMC
FPGA_Switch1
PINdiode
Header_P5



TITLE: Tunable Laser driver

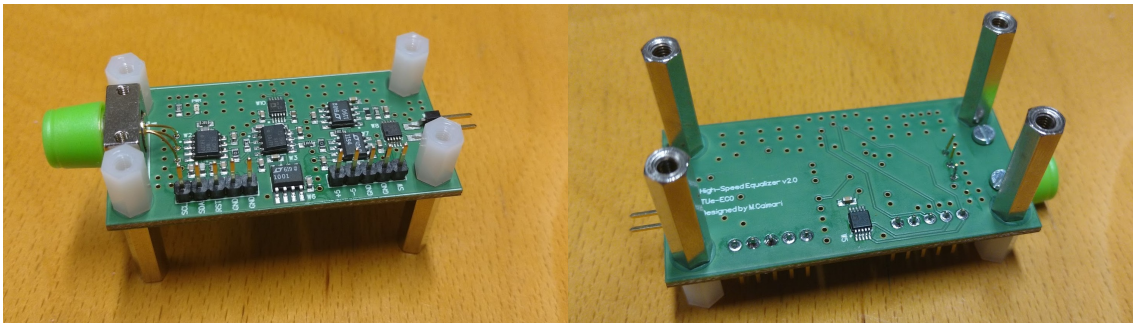
SIZE	DWG NO	REV
A3	SOA, Phase Module Driver	0

DRAWN BY	SCALE	SHEET	
Miquel Caimari		3 of 3	14/12/2016:16:45


U1
PINdiode
1VEE
PD+
CASE
3 GND
PD-
2
C1 170f J1_IN
R1 50k
OPA847
NC0
-IN
+IN
VEE
_DIS
VDD
OUT
NC1
U2
50k
R2
C10 100n
C11 100p
VEE
C4 31p
C3 680p
R5 60
J1_OUT
R4 100
OPA847
U3
J2_IN
R7 2k
C16 12p
LT1190
BAL0
BAL1
U7
J2_OUT
R8 6
LT1194CS8
REF
U4
R9 50
Jumper_SMC
IN
OUT
U9
FPGA_Switch
TS5A23160
IN1
NO1
GND
NO2
IN2
COM1
NC1
NC2
COM2
U8
R39 1k
U28
LT1001CS8
OFFS
OFFS1
NC
U6
3214X_Potentiometer
P1
P2
P3
P4
P5
FPGA_SWITCH
Header_P5
R3 0
R6 0
C6 C13 C5 C14 C17 C12 C2 C9 C8 C15 C7
100n
TITLE
High-Speed Equalizer v1.0
SIZE
A4
DWG NO
Fixed Values, Slope = 0,6
REV
0
DRAWN BY
Miquel Caimari
SCALE
SHEET
1
of
3
28/11/2016:14:22

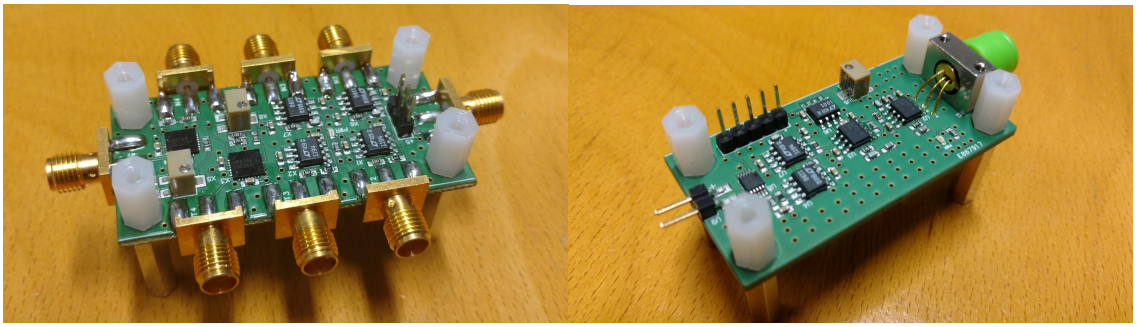
Appendix C

Prototypes



(a) Top-view, High-Speed Equalizer v2.0 (b) Bottom-view, High-Speed Equalizer v2.0

Figure C.1: Full-flexible configuration, High-Speed Equalizer v2.0



(a) Tunable Laser Driver (b) Top-view, High-Speed Equalizer v1.0

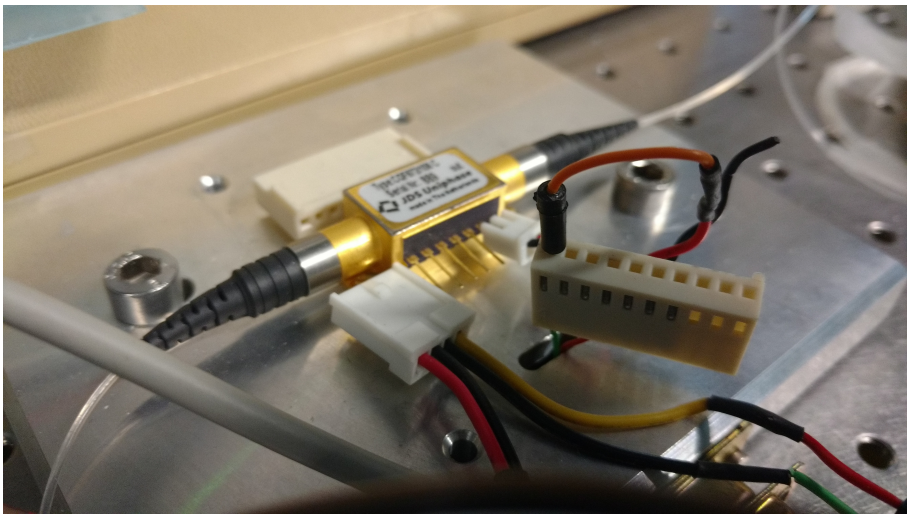
Figure C.2: Tunable Laser Driver and High-Speed Equalizer v1.0

Table C.1: Final value of the components

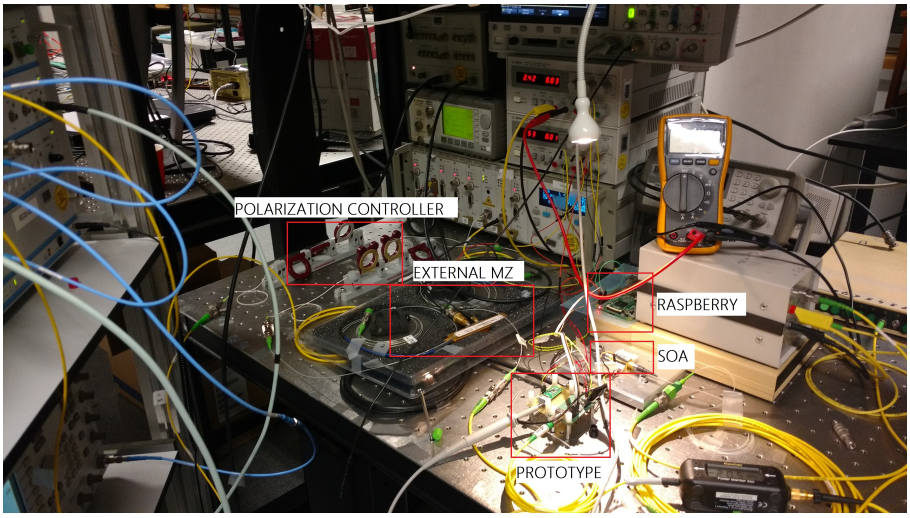
#	QTY	Part Number	Value	Ref Designator
1	2	C0603	170f	C1,C18
2	38	C0603	100n	C2,C5-C10,C12-C15,C17,C19,C21,C24-C28,C30-C34,C36,C37,C40-C51
3	1	C0603	680p	C3
4	1	C0603	31p	C4
5	2	C0603	100p	C11,C29
6	4	C0603	12p	C16,C35,C38,C39
7	1	C0603	9p6	C20
8	1	C0603	1p2	C22
9	1	C0603	1u	C23
10	3	Header_P5	P1-P3	
11	4	R0603	50k	R1,R2,R10,R11
12	8	R0603	0	R3,R6,R12,R15,R30,R31,R34,R35
13	1	R0603	100	R4
14	1	R0603	60	R5
15	4	R0603	2k	R7,R16,R19,R22
16	2	R0603	3	R8,R17
17	6	R0603	50	R9,R18,R21,R24,R26,R33
18	1	R0603	10k	R13
19	1	R0603	40	R14
20	2	R0603	2	R20,R23
21	2	R0603	165	R25,R32
22	2	R0603	3k	R29,R38
23	3	R0603	1k	R39-R41
24	2	PINdiode	U1,W1	
25	4	OPA847	U2,U3,W2,W3	
26	4	LT1194CS8	U4,W4,X1,X2	
27	3	3214X_Potentiometer	U5,X5,X8	
28	2	LT1001CS8	U6,W6	
29	4	LT1190	U7,W7,X6,X7	
30	2	TS5A23160	U8,W8	
31	2	Jumper_SMC	U9,W9	
32	8	SMA	U17-U24	
33	1	Header_P3	U27	
34	3	LED	U28-U30	
35	1	AD5259	W5	
36	1	AD5270	W10	
37	2	LMH6525	X3,X4	

Appendix D

Laboratory's pictures



(a) SOA connection



(b) Setup for the experiments

Figure D.1: Pictures of the laboratory

Appendix E

Software source code

E.1 AD5272 - Rheostat

```
import smbus
from time import sleep  # this lets us have a time delay (see line 12)
import RPi.GPIO as GPIO
import quick2wire.i2c as i2c

# for GPIO numbering, choose BCM
GPIO.setmode(GPIO.BCM)
GPIO.setup(24, GPIO.OUT)

# Disabling RESET PIN
GPIO.output(24, 1)  # set GPIO24 to 1/GPIO.HIGH/True

# AD5272 POTENTIOMETER METHODS
address = 0x2e

# Adafruit I2C


# Command Instructions
# NOP: do nothing
command1 = 0x00
# Write contents of serial register data to RDAC.
command2 = 0x04
# Read contents of RDAC wiper register.
command3 = 0x08
# Store wiper setting: store RDAC setting to 50-TP.
command4 = 0x0C
# Software reset: refresh RDAC with the last 50-TP memory stored value.
command5 = 0x10
# Read contents of 50-TP from the SDO output in the next frame.
command6 = 0x14
# Read address of the last 50-TP programmed memory location
command7 = 0x18
# Write contents of the serial register data to the control register.
command8 = 0x1C
# Read contents of the control register
command9 = 0x20
# Software shutdown.D0 = 0; normal mode. D0 = 1; shutdown mode
command10 = 0x24


# Read Operations
def R_from_RDAC(variables):
    with i2c.I2CMaster() as bus:
        read_results = bus.transaction(
            i2c.writing_bytes(address, command3, 0x00),
```

```
            i2c.reading(address, 2))
    MSB = read_results[0][0]
    LSB = read_results[0][1]
    byte = MSB * pow(2, 8) + LSB
    return byte


def R_from_50TP(variables):
    with i2c.I2CMaster() as bus:
        read_results = bus.transaction(
            i2c.writing_bytes(address, command7, 0x00),
            i2c.reading(address, 2))
    TPvalue = read_results[0][1]
    return TPvalue


def R_from_Rcontrol():
    with i2c.I2CMaster() as bus:
        read_results = bus.transaction(
            i2c.writing_bytes(address, command9, 0x00),
            i2c.reading(address, 2))
    RDACmask = read_results[0][1]
    return RDACmask


# Write operations

def write_op(command, variables):
    value_INT = int(variables['data'])

    if value_INT < 256:
        commandbus = command
        value = value_INT

    elif 256 <= value_INT < 1024:

        bin_value = bin(value_INT)[2:len(bin(value_INT))]
        if value_INT < 512:
            commandbus = command + int(bin_value[:1], 2)
            value = int(bin_value[1:len(bin_value)], 2)

        else:
            commandbus = command + int(bin_value[:2], 2)
            value = int(bin_value[2:len(bin_value)], 2)

    with i2c.I2CMaster() as bus:
        bus.transaction(i2c.writing_bytes(address, commandbus, value))


def W_to_RDAC(variables):
    write_op(command2, variables)


def W_to_RControl(variables):
    write_op(command8, variables)


# Special Instructions
def NOP():
    with i2c.I2CMaster() as bus:
        bus.transaction(i2c.writing_bytes(address, command1, 0x00))
        # bus.write_byte(address, command1)


def Restore_to_RDACWiper(variables):
    with i2c.I2CMaster() as bus:
        bus.transaction(i2c.writing_bytes(address, command4, 0x00))
```

```
        # bus.write_byte(address, command4)
        # NOP()


def Store_to_50TP(variables):
    with i2c.I2CMaster() as bus:
        bus.transaction(i2c.writing_bytes(address, command3, 0x00))

        # bus.write_byte(address, command3)
        # return R_from_Rcontrol()


# Control Register operations:
def RPerformance(variables):
    flag_Performance = str_to_bool(variables['flag'])
    value = R_from_Rcontrol()
    if flag_Performance:
        ONvalue = value | 0x4
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, ONvalue))
            # bus.write_byte_data(address, command8, ONvalue)
            # R_from_Rcontrol()
    else:
        OFFvalue = value & 0x3
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, OFFvalue))
            # R_from_Rcontrol()


def RDAC_protection(variables):
    flag_protection = str_to_bool(variables['flag'])
    value = R_from_Rcontrol()

    if flag_protection:
        ONvalue = (value | 0x2)
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, ONvalue))
            # bus.write_byte_data(address, command8, onvalue)

    else:
        OFFvalue = value & 0x5
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, OFFvalue))
            #   bus.write_byte_data(address, command8, OFFvalue)


def TP_enable(variables):
    flag_enableTP = str_to_bool(variables['flag'])
    value = R_from_Rcontrol()
    if flag_enableTP:
        ONvalue = value | 0x1
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, ONvalue))
            # bus.write_byte_data(address, command8, ONvalue)
            # R_from_Rcontrol()
    else:
        OFFvalue = value & 0x6
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command8, OFFvalue))
            # bus.write_byte_data(address, command8, OFFvalue)
            # R_from_Rcontrol()


def power_control(variables):
    flag_power = str_to_bool(variables['flag'])

    if flag_power:
```

```
        ONvalue = 0x00
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command10, ONvalue))
        # bus.write_byte_data(address, command10, ONvalue)
        return True
    else:
        OFFvalue = 0x01
        with i2c.I2CMaster() as bus:
            bus.transaction(i2c.writing_bytes(address, command10, OFFvalue))
        # bus.write_byte_data(address, command10, OFFvalue)
        return False


def softreset(variables):
    with i2c.I2CMaster() as bus:
        bus.transaction(i2c.writing_bytes(address, command5, 0x00))
        # bus.write_byte(address, command5)


def hardreset(variables):
    GPIO.output(24, 0)  # set GPIO24 to 1/GPIO.HIGH/True
    sleep(0.5)  # wait half a second
    GPIO.output(24, 1)


def str_to_bool(s):
    if s == 'true':
        return True
    elif s == 'false':
        return False
    else:
        raise ValueError  # evil ValueError that doesn't tell you what the wrong
            value was


def Binary_to_Hex(byte):
    hex_number = hex(byte)
    return hex_number
```

E.2 AD5259 - Potentiometer

```
import smbus
import time
import os
from fcntl import ioctl
from ctypes import c_uint32, c_uint8, c_uint16, POINTER, Structure, Array, Union
# AD5259 POTENTIOMETER METHODS
bus = smbus.SMBus(1)
address = 0x18

# Command Instructions
# Operation Between Interface and RDAC.
command1 = 0x00
# Operation Between Interface and EEPROM.
command2 = 0x20
# Operation Between Interface and Write Protection Register.
command3 = 0x40
# NOP
command4 = 0x80
# Restore EEPROM to DAC
command5 = 0xA0
# Store RDAC to EEPROM
command6 = 0xC0
```

```
def Read_from_RDAC(variables):
    RDACvalue = bus.read_byte_data(address, command1)
    #rtest = bus.read_byte(address)
    return RDACvalue


def Read_from_EEPROM(variables):
    EEPROMvalue = bus.read_byte_data(address, command2)
    return EEPROMvalue


# Generic write method:
#

def write_op(command, variables):
    value_INT = int(variables['data'])
    bus.write_byte_data(address, command, value_INT)


def Write_to_RDAC(variables):
    write_op(command1, variables)


def Write_to_EEPROM(variables):
    write_op(command2, variables)


def WP_mode(variables):
    write_op(command3, variables)


def NOP(variables):
    bus.write_byte(address, command4)


def Restore_to_RDAC(variables):
    bus.write_byte(address, command5)
    NOP(variables)


def Store_to_EEPROM(variables):
    bus.write_byte(address, command6)



def Binary_to_Hex(byte):
    hex_number = int(byte, 2)
    return hex_number


def manual_mode(variables):
    commandIN = Binary_to_Hex(variables['command'])
    dataIN = Binary_to_Hex(variables['data'])
    bus.write_byte_data(address, commandIN, dataIN)


def read_from_slave(variables):
    return bus.read_byte(address)
```